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CMOS FREQUENCY MIXERS FOR APPLICATION IN THIRD GENERATION W-CDMA RECEIVERS

BY

SU TARN LIM ©

A THESIS

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The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies and Research for acceptance, a thesis entitled CMOS Frequency Mixers for Application in Third Generation W-CDMA Receivers submitted by Su Tarn Lim in partial fulfillment of the requirements for the degree of Master of Science

Abstract

Two architectures of CMOS frequency mixers—switching and multiplying are presented. For the proposed switching mixer, two pairs of transistors are switched on and off alternatively at the frequency of a local oscillator, generating a square wave. Frequency translation is facilitated by the modulation of the input signal with the generated square wave. In contrast, the multiplier mixer proposed is an active load Gilbert multiplier cell that achieves the frequency translation by multiplying the input signal with a local oscillator signal. The work in this thesis involves a module to be used as the receiving link at the front-end of a third-generation code division multiple access wireless system. The feasibility of such a transceiver on a single chip in a 0.18μm CMOS environment was investigated. Two mixer modules with the aforementioned architectures have been designed, fabricated, and tested using performance measures such as voltage conversion gain and linearity as a guide. Theoretical analyses of conversion gain were verified using software simulations, while the linearity performances were taken experimentally. A discussion is presented to account for discrepancies between the actual results and theoretical expectations such as the lower-than-expected conversion gains, third intercept and 1dB points for both mixers modules.

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List of Symbols

C	capacitor
C_b	DC-blocking capacitor
C_{OX}	gate oxide capacitor
E_{SAT}	saturation field
G	conversion gain
f	frequency
f_{LO}	local oscillator frequency
f_{IF}	intermediate frequency
g_m	transistor transconductance
I	current
I_{BIAS}	bias current
I_{DS}	drain-source current of MOS transistor
L	length of MOS transistor gate
L_{IND}	inductor
L_{CRIT}	minimum length of MOS transistor gate to avoid short-channel effect
n	number of turns of inductor
NF	noise figure
P	pitch of square spiral on-chip inductor
r	radius of square spiral on-chip inductor
R_{BIAS}	bias resistor
R_{DIODE}	diode resistor
R_{DS}	series resistance of MOS transistor
R_{ON}	resistance of MOS transistor serving as active load
R_{SOURCE}	input resistance
SNR	signal-to-noise ratio

t	Time
T_{OX}	oxide thickness
V	voltage
V_{BIAS}	bias voltage
V_{CC} (V_{DD})	voltage power supply
V_{DS}	drain-source voltage
V_{GS}	gate-source voltage
V_{IF}	intermediate frequency voltage
V_{LO}	local oscillator voltage
V_{RF}	radio frequency voltage
V_T	threshold voltage
W	width of MOS transistor gate
Z_{LOAD}	load impedance
ω	radian frequency
μ	mobility of charge carriers

Chapter I

1.0 Introduction

Electronic wireless communication has been around for the last fifty years; however, the development growth in the area had been relatively slow. In the last decade, there has been a renewed interest in wireless applications. This renewed interest is the direct result of consumer demand for better performance from cellular telephones, two-way pagers, and cordless telephones. To meet the growth in the wireless telecommunication market, many manufacturers initiated new research in hope of developing wireless transceivers that are low-cost, small in size, and low in power consumption [1]. Most of the wireless networks that are being deployed currently operate around 1 GigaHertz (GHz) frequency. However, with new spectrum allocated for the Bluetooth and the Third-Generation Cellular Systems (3G) [2-4], many new applications are also being proposed (e.g., wireless video on demand). To perform these new applications proposed for Bluetooth and 3G, better performance transceivers that operate at low power are needed.

Since the first mobile transceiver was introduced, numerous different design methodologies have been implemented. However, all mobile wireless transceivers can be viewed in basic building-block form as shown in Figure 1-1. As seen in Figure 1-1, the antenna is connected to the low noise amplifier or the power amplifier depending an whether the transceiver is in receiving or transmitting mode. In the receiving path, the radio-frequency (RF) signal is first filtered by the RF filter to the remove undesired noise.

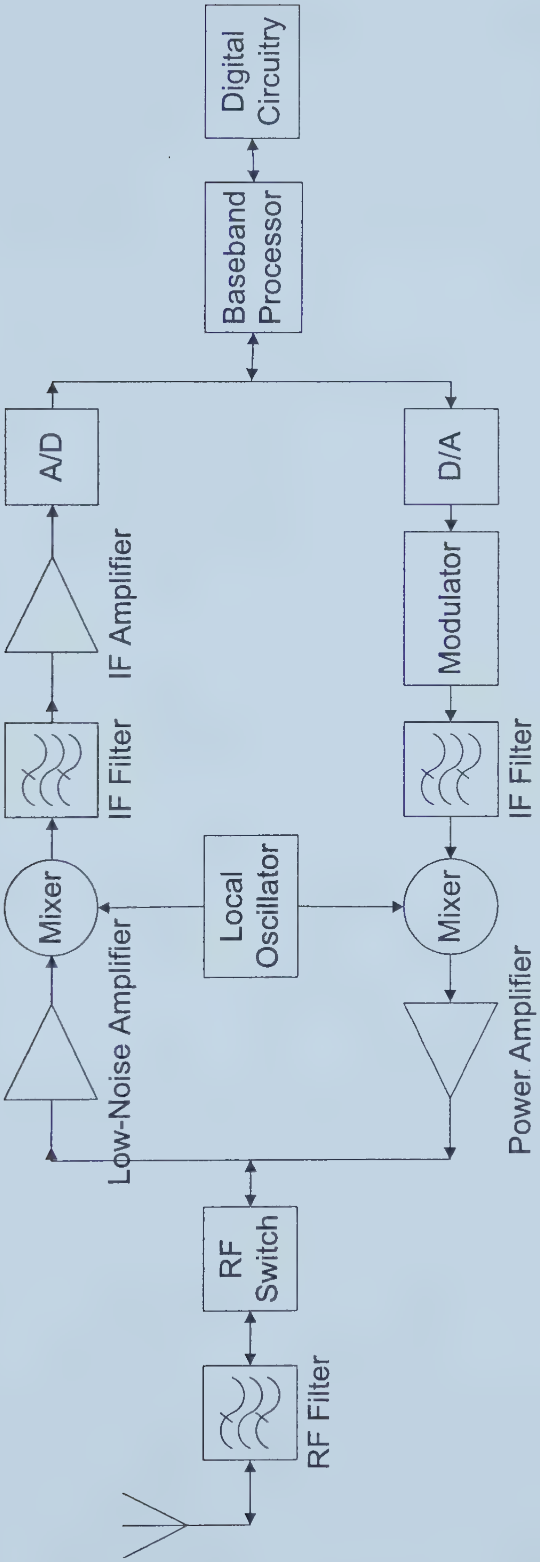


Figure 1-1: Typical Building Blocks of Mobile Wireless Transceiver.

In receiving mode, a low noise amplifier (LNA) amplifies this filtered signal. After amplification, the RF signal is passed through a frequency mixer. Together with the local oscillator (LO), the frequency mixer translates the frequency of the incoming signal. The output of the mixer is filtered to obtain the intermediate-frequency (IF) signal while removing all spurious responses and noise. Finally, an IF amplifier amplifies the signal before the signal transverses through an analog-digital converter (A/D) to be converted into a digital signal for baseband processing. In the transmitting path, the information bits are converted from digital bits into analog signals, modulated at low frequency. In order to facilitate the propagation of signals, the modulated signals are frequency translated to higher frequencies. Then, at the subsequent stages, a power amplifier is used to boost the signal level for transmission via the antenna.

Numerous technologies are available for hardware implementation, including Gallium Arsenide (GaAs), Silicon Bipolar, Complementary Metal-Oxide-Semiconductor (CMOS), and Silicon Germanium (SiGe). The choice of technology used in each module is generally influenced by several factors such as cost of fabrication, switching speed, nonlinear properties, and frequency of operation. In a large number of situations, different technologies are used for fabrication processes of different building blocks for the transceiver unit.

Traditionally, switches are fabricated using GaAs technology whereas amplifier and mixer are often fabricated using Silicon Bipolar technology; finally, D/A and A/D converters are fabricated using CMOS technology. The practice of using different technologies for different modules resulted in larger devices, higher manufacturing cost, and the need to solder the numerous chips onto printed circuit board (PCB). In addition,

the micro-strips used to connect the stages degrade the performance of the whole system. One of possible solution to avoid the need of soldering and higher than necessary manufacturing cost would be to manufacture the whole device in one fabrication run using one single type of technology.

For many years, numerous proposals have been put forward as to which technology to be used for the single-chip transceiver. The advancements in CMOS technology over the last two decades gave rise to lower noise figures and faster switching speeds [5-10]. These advances in CMOS technology and new design methodologies in designing transceivers that are simple and dependable led to the possibility of creating an all-CMOS transceiver in an end-to-end solution. These all-CMOS transceivers offer the possibility of using single transceiver chip. This is a very attractive attribute that offers a favorable price versus performance in front-end radio frequency modules as it lowers cost and can be manufactured together with the digital baseband circuit.

1.1 Frequency Mixer, Is It a Necessity?

To produce frequencies that do not exist at the input, mixers must possess nonlinear characteristics. Abundant devices exhibit nonlinear properties when operating in diverse environments; however, some of these devices exhibit noise and spurious responses that are objectionable (for example, vacuum tube and a pair of rusty scissor have nonlinear properties but provides poor conversion gain, linearity, and isolation when operate as frequency mixers). The choice of the device selected to operate as a frequency mixer will help in determining the overall performance of a wireless system. Frequency mixer is often used to translate high frequency signals to low frequency signals (down conversion)

at the receiver, whereas they are used to convert low frequency signals to high frequencies (up conversion) at the transmitter [11].

Often the question is asked, as to why do we need frequency mixers when broadband and narrowband amplifiers centered at different frequencies can be readily designed and implemented? The use of a frequency mixer eases tuning and selectivity—filters with fixed-frequencies that are much easier to realize than variable-frequency filters and amplifiers. Another reason why mixers are used is due to the limited quality factor (Q-factor) for filters of high frequency. Bandwidth, center (or carrier) frequency, and Q-factor of simple band-pass filters are related to each other as shown below,

$$Bandwidth = \frac{\omega_{carrier}}{Q - factor} . \qquad (1.1)$$

From (1.1), good quality filters with a high Q-factor are required to maintain the required bandwidth for high frequency filters. For instance, with a 900MHz carrier frequency and a 5MHz bandwidth, filters with a Q-factor of 180 would be needed. This is rather difficult, if not impossible to realize. On the other hand, if the same carrier signal is preliminary shifted to operate at a lower frequency of 125MHz, for the same bandwidth, filters with a Q-factor of 25 can be used instead to provide the same selectivity.

To obtain higher wave propagation efficiency and the ability to multiplex numerous information-containing signals onto one carrier to be sent simultaneously, the transmitted carrier frequency has to be increased. However, frequency mixers are used in wireless systems to maintain similar overall selectivity [12]. The increase in the carrier frequency and the hope of using a single chip transceiver had increased the importance of the frequency mixer. With the maximum obtainable Q-factor of 10 in CMOS technology

[13], to maintain good selectivity in a transceiver, frequency mixers are often needed. Mixers are used to shift the frequency close to baseband such that amplification, modulation, and demodulation can be performed more easily before and after the frequency shift in the receiver and transmitter respectively.

1.2 Thesis Content

This thesis investigates two frequency mixers of different architectures - switching and multiplying mixers. These architectures have been designed, fabricated, and tested using 0.18μm CMOS technology. To the best of this author's knowledge, no work using 0.18μm CMOS technology for the implementation of frequency mixers has appeared in the literature. Therefore, an investigation has been carried out to determine if RF front-end modules can be constructed which have better performance characteristics for the 3G Cellular Telephony using the new CMOS technology.

Chapter 2 presents the metrics that are used to assess the performances of mixers, while Chapter 3 presents the basics of the operation of mixers for the two different categories. Examples of two types of frequency mixers are also presented at the end of Chapter 3. Chapter 4 focuses on the manufactured mixers, documentation regarding the design, simulation results, and experimental results of two CMOS frequency mixers. Relevant calculations are also included in Chapter 4. Finally, Chapter 5 summarizes what was conducted and presented in this thesis, and concludes the thesis by providing some suggestions for future research.

Chapter 2

2.0 Introduction to Performance Metrics

Signal paths in transmitters and receivers both contain at least one frequency mixer with which to perform frequency conversion. During the frequency conversion operation, a nonlinear device is used to create a signal of frequency spectrum not present at the input. All nonlinear devices that are used as mixers share a common attribute, namely the multiplication of two signals in the time domain generates a shift in the frequency spectral components. The sum and the difference frequency components ($\omega_1 \pm \omega_2$) are produced via analog multiplication. This can be understood from the trigonometric identity,

$$(A\sin\omega_1 t)*(B\sin\omega_2 t)=\frac{AB}{2}\left[\cos(\omega_1-\omega_2)t-\cos(\omega_1+\omega_2)t\right]. \tag{2.1}$$

As relevant technology and design methodologies were developed, frequency mixers of numerous different designs had been created. Characterization of these different mixers was needed together with a basis with which to evaluate the performances among the different architectures [14]. This chapter provides an in-depth view of these performance metrics.

Just as in other fields such as photonics, networking, digital integrated circuits, and telecommunications, the design of frequency mixers requires the knowledge of performance metrics that include some basic definitions and terminologies. The list of

metrics used to judge a mixer's quality are as follows: conversion gain, linearity, power consumption, noise figure, and isolation.

2.1 Conversion Gain

One of the most important characteristics and commonly used performance metrics for frequency mixers is conversion gain (or loss). It measures the ratio of the desired IF output to the RF input. In (2.1), assuming A and B are the amplitudes of the RF and LO signals respectively, the multiplication generates a desired IF signal with an amplitude of AB/2. Performing the conversion gain calculation by dividing the desired IF signal by the RF signal results in B/2 or half the LO amplitude.

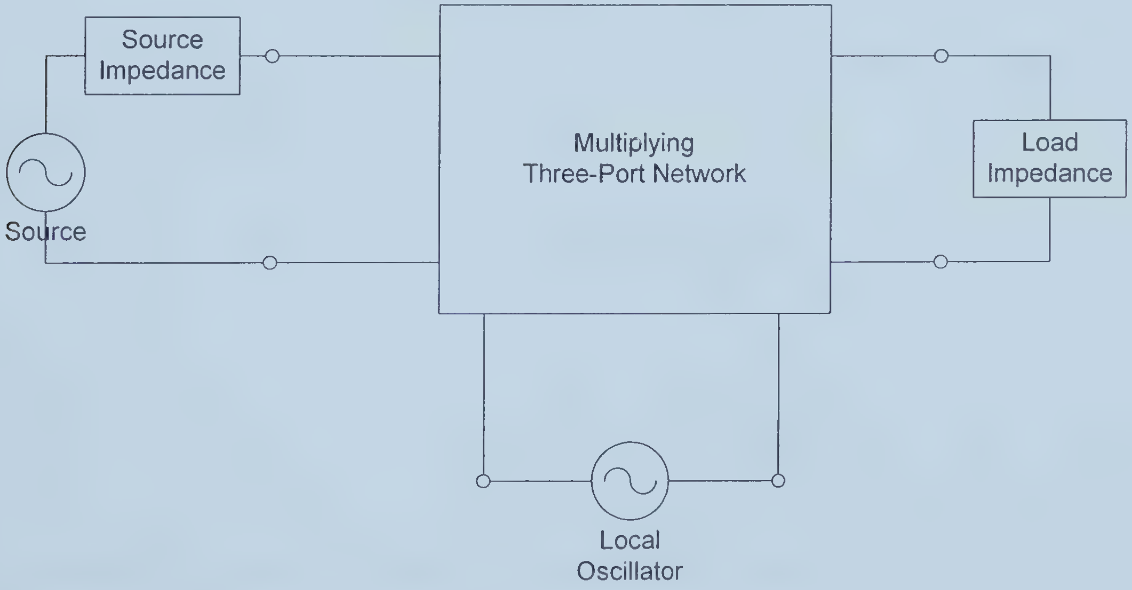


Figure 2-1: Three-Port Network for Definition of Conversion Gain

Figure 2-1 shows a generic configuration of a three-port network representing a mixer under test. With this figure, we will illustrate the concept of conversion gain. When the load impedance is real, power conversion gain can be used for characterization. Power

conversion gain, G_α, parameter used in matching theory is defined as the power delivered to the load divided by the power available from the source:

$$G_\alpha = \frac{Power\ Delivered\ to\ the\ Load}{Power\ Available\ \ from\ Source}. \tag{2.2}$$

Conversely, when the load impedance is purely imaginary, power cannot be measured; voltage conversion gain must be evaluated instead. Power conversion gain is invalid when the load impedance is purely imaginary as the average power delivered to the reactive load is zero. Voltage conversion gain, G, is defined as the voltage amplitude across the load divided by the voltage amplitude across the source:

$$G = \frac{Voltage\ Ampltitude\ Across\ Load}{Voltage\ Ampltidue\ Across\ Source}. \tag{2.3}$$

Both power and voltage conversion gain can be expressed in logarithmic format. The formulations are shown in (2.4) and (2.5) below:

$$G_\alpha(dB) = 10\log\left(\frac{V_O}{V_i}\right)^2. \tag{2.4}$$

and

$$G(dB) = 20\log\left(\frac{V_{O,RMS}}{V_{i,RMS}}\right). \tag{2.5}$$

Frequently, the power of a signal is expressed in dBm based on the following formulation:

$$Signal\ Power(dBm) = 10\log_{10}\frac{Power}{1mW}. \tag{2.6}$$

Conversion gain in excess of unity is often convenient since the mixer provides not only frequency conversion but also amplification. A mixer with amplification is desirable

because it provides a stronger output signal relative to the noise generated in the signal path and it adds to the possibility of reducing the gain of subsequent amplifier stages.

2.2 Distortion and Linearity

The ideal mixer would have a linear relationship between RF-input power and IF-output power for all ranges of values. However, for virtually all physical systems, this does not always hold true. The nonlinearity in devices used can produce signals containing frequency spectrum that are same as that of the desired signals [14]. The mixer nonlinearities that are of the greatest concern are those of third order. The mixer nonlinear behavior parameters are obtained by approximating mixer characteristic by a third order nonlinear polynomial. The output of a nonlinear device, $V_{Out,}$ can be related to its input, V_{IN}, as follows:

$$V_{Out} = a_0 + a_1 * V_{IN} + a_2 * V_{IN}^2 + a_3 * V_{IN}^3 + \dots \tag{2.7}$$

where a_0, a_1, a_2, and a_3 are the coefficients of the DC term, first, second and third order terms respectively.

Assume the input signal V_{IN} is the sum of two sinusoidal signals, i.e.

$$V_{IN} = A\cos\omega_1 t + B\cos\omega_2 t\,. \tag{2.8}$$

The results shown in (2.9) occur when (2.8) is substituted into (2.7). The first and second terms in (2.9) are often situated far away from the desired output in the frequency spectrum and are often easily filtered. The square term in (2.9) produces the desired signal and its image,

$$\begin{aligned} V_{Out} &= a_0 + a_1(A\cos\omega_1 t + B\cos\omega_2 t) + a_2(A\cos\omega_1 t + B\cos\omega_2 t)^2 \\ &+ a_3(A\cos\omega_1 t + B\cos\omega_2 t)^3 + \dots \end{aligned}\,. \tag{2.9}$$

If the nonlinear device is characterized by a second order equation, filtering of any undesirable signal and noise could be easily done. However, the influence of the cubic term in (2.9) highlighted in (2.10) shows that this is not the case. Expansion of the cubic term in (2.10) clearly shows that it is possible to obtain IF frequencies from signals other than the desired RF signal from the last group of terms in (2.10), even if the unwanted signal is very far from the RF signal in the frequency spectrum. More specifically, any responses in the frequency mixer with frequency components connected by the relationships $2\omega_1-\omega_2=\omega_{IF}$ or $2\omega_2-\omega_1=\omega_{IF}$ will produce a response at the output that occupy the same frequency spectrum as the desired term.

$$\begin{aligned} a_3(A\cos\omega_1 t + B\cos\omega_2 t)^3 &= \frac{3a_3}{2}\left(AB^2+\frac{A^3}{2}\right)\cos\omega_1 t + \frac{3a_3}{2}\left(A^2B+\frac{B^3}{2}\right)\cos\omega_2 t \\ &+\frac{a_3}{4}\left[A^3\cos 3\omega_1 t + B^3\cos 3\omega_2 t\right] \\ &+\frac{3a_3AB}{4}\left[A\cos(2\omega_1+\omega_2)t + B\cos(2\omega_2+\omega_1)t\right] \\ &+\frac{3a_3AB}{4}\left[A\cos(2\omega_1-\omega_2)t + B\cos(2\omega_2-\omega_1)t\right] \end{aligned} \quad . \qquad (2.10)$$

For example, if the LO frequency f_{LO} = 850 KHz and the IF frequency f_{IF} = 150 KHz, the down conversion mixer will respond not only to the desired RF signal with (850 ± 150) KHz that are produced by the square term in (2.9), but also it would respond to any signals with a frequency of 500 KHz. The desired output will be distorted by the signals with frequency component of 500 KHz as $2f_{RF}-f_{LO}$=2x500-850 = 150 KHz.

Looking at (2.10), it is evident that as the input power level increases, the output signal level will also increase. However, starting at sufficiently high input power, the coefficient

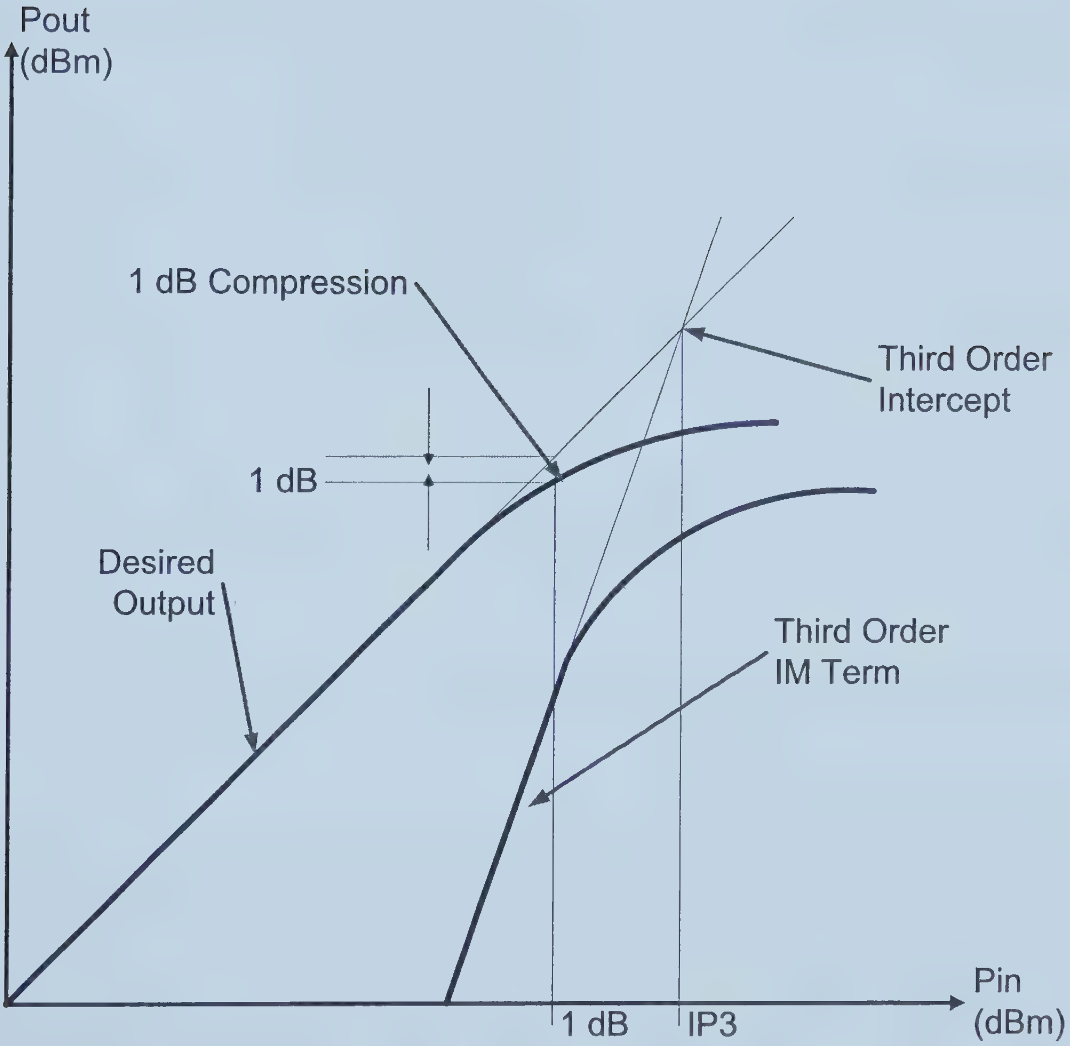


Figure 2-2: Definition of Mixer Linearity Parameters

of the cubic term in (2.10) starts to rise rapidly and becomes larger than the coefficient of the square term in (2.9), making the inequality in (2.11) to become true.

$$\frac{a_2 AB}{2} \leq \frac{3a_3 A^2 B}{4}. \tag{2.11}$$

When (2.11) is valid, the cubic term will start to distort the intermediate frequency output and the output will no longer be proportional to the input.

To avoid the distortion, the input amplitude used in testing is often kept low to determine the dynamic limit for the input power level. Unfortunately, the values of a_2 and a_3 of a module block in (2.9) are often unknown, making theoretical calculation impossible such that it can only be inferred from measurements. The distortion due to this cubic term is called two-tone third-order intermodulation. It is used to characterize mixer linearity.

Another linearity parameter that is often associated with mixer is the compression point. Usually, both the fundamental and cubic term compress and deviate from linearity at high input power. The 1dB compression point relates to the RF input power level above which the IF output versus RF input power is reduced by 1dB from the linear characteristic [15].

The test procedure to measure the intermodulation is done in two steps. First, values of IF power readings are taken as two signals with RF and LO frequencies are applied to the mixer. The second step involves taking the output IF power reading with the application of a signal with frequency ω_1 and LO signal such that $2\omega_1 - \omega_{LO} = \omega_{IF}$. In both steps, the IF starts to grow with increased input power level, but it starts to compress at higher input power levels due to the limitations of real devices. Due to the compression, the third order intercept point is usually found by extrapolation. These concepts are summarized in Figure 2-2.

2.3 Noise Figure

Noise figure is a measure of how much noise is introduced to the signal by the module. It refers to the signal-to-noise ratio (SNR) at the input (RF) port divided by the SNR at the output (IF) port. This is illustrated in (2.12):

$$\text{Noise Figure (NF)} = \frac{\text{Input SNR}}{\text{Output SNR}}. \tag{2.12}$$

Two types of noise figures are often defined in mixers: single sideband (SSB) and double sideband (DSB). The SSB noise figure contains only the noise power from the noise power of the RF components while the noise power of the image component is discarded. On the other hand, the DSB noise figure includes both the noise power of the IF component and the noise power of the image component. Generally, there is no desired signal at the image frequency resulting in better noise figure values when SSB noise figures are quoted.

When comparing noise figures in the mixer to other stages of the signal path, the values are regularly higher than for the other stages. This happens because any noise from frequencies other than desired RF is often mixed down, third-order intermodulation effects, and appear as noise at the output.

2.4 Isolation

Isolation defines the fraction of power that leaks to other ports. There is no absolute isolation between the ports due to the parasitic coupling between any two ports. Generally, it is desirable to minimize interaction among the RF, IF, and LO ports, and this is especially true for IF-RF isolation. Since the LO signal power is generally quite large compared to that of the RF signal power, any LO fed through to either RF port can

cause undesirable results at later stages of the signal paths. This is apparent if any of the LO signal power is leaked into the RF port. The leaked power will mix with the LO signal itself through the mixer operation, resulting in a DC offset at the IF output. The situation becomes worse if any two of the three signals have frequencies that are close to each other, rendering the process of filtering ineffective.

The common practice of measuring isolation is carried out by applying a signal at one of the three ports, with a second port short-circuited. The influence of the applied signal is measured at the third port to determine the isolation between the first and third port. This process is repeated to determine the isolation between all combinations of any two ports.

2.5 Power Consumption

With the introduction of mobile multimedia, power consumption of battery-powered cellular system becomes a design issue. In order to minimize the size and weight while maintaining an acceptable battery life, power consumption becomes an important performance metric design issue. The power consumption of mixer modules is required to be as low as possible. Similar to other modules in radio frequency front-ends, power consumption by mixer operation is often quoted and listed. The quoted number often accounts for power dissipated in the mixer core and does not include the LO power used at the LO port.

Chapter 3

3.0 Introduction to Mixer

Mixer performance parameters were introduced in the previous chapter. These metrics are often used in the evaluation and comparison of various mixers. A large number of different frequency mixers have appeared in the literature over the last few decades as a result of varieties of design methodologies; however a review of the literature list suggests that all mixers can be classified into two categories—Switching and Multiplier mixers.

The two categories of mixers provide frequency translation. Yet, they differ in how the output signal is created. For mixers that are categorized as switching, the output signals are produced when the input signals are modulated or multiplied by a square wave. On the other hand, for the mixers that are categorized under the multiplier group, the input signals are multiplied with the local oscillator signal to produce the desired IF component.

In this chapter, the above two different architectures for mixers will be presented. Basic operation of each type as well as the differences between all of the different designs will be discussed in remaining part of the chapter.

3.1 Switching Mixer

Some similarities can be observed for all switching mixers. One of the main characteristics of switching mixers is that switches are implemented as time-varying

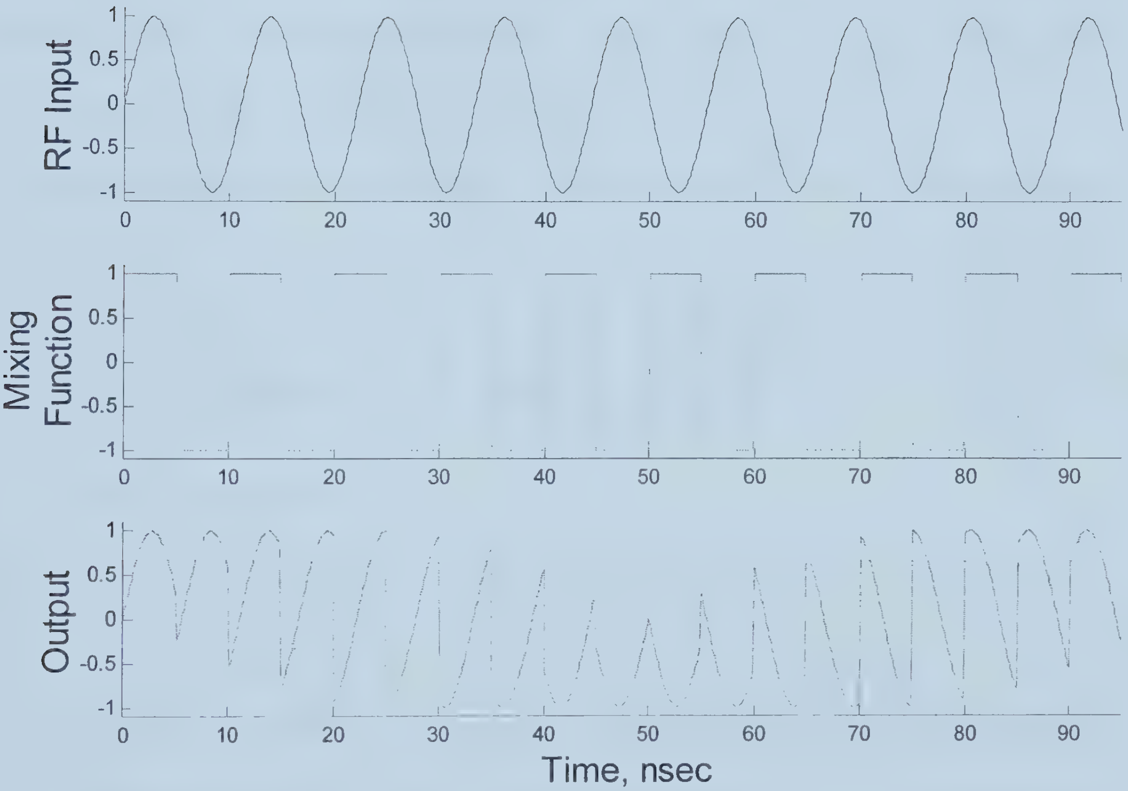


Figure 3-1: Principle of Operation of Switching Mixer in Time Domain.

circuit elements using diodes or transistors. A demonstration of the principle of operation for switching-based frequency mixers is illustrated in Figure 3-1.

In the figure, an input sinusoidal signal of frequency 90MHz is multiplied by the mixing function, a unit square signal, of frequency 100MHz. The output produced contains two frequency components—the sum and the difference of the input and mixing function. The performance parameter of low-power operation can often be associated with a switching mixer [12]. This is a highly desirable feature especially when the mixer is implemented in mobile cellular systems that operate with low power.

A traditional and simple implementation of a mixer would be the two-diode switching mixer. From this simple circuit further improvements can be made using different arrangements of transformers and more diodes or transistors. Schematic and mixing operation for these switching mixers will be discussed below.

3.1.1 Two-Diode Switching Mixer

This mixer design is often found in textbooks to provide a fundamental understanding of mixer operation. A basic schematic showing the setup of the circuit is given in Figure 3-2. Assuming that the transformer is ideal and that sinusoidal LO source is significantly larger than the sinusoidal RF signal, the two diodes switch on and off depending on the phase of the LO signal. The switching effect produces a 180° change in the RF signal appearing at the load impedance. When quantified mathematically, the output is as given by (3.1)

$$Vout(t) = \begin{array}{ll} V_{RF}(t) + V_{LO}(t) & \text{when } V_{LO}(t) > 0 \\ -V_{RF}(t) + V_{LO}(t) & \text{when } V_{LO}(t) < 0 \end{array}. \tag{3.1}$$

The periodic 180° change in the RF signal can be represented by a $V_{RF}(t)$ multiplied by a

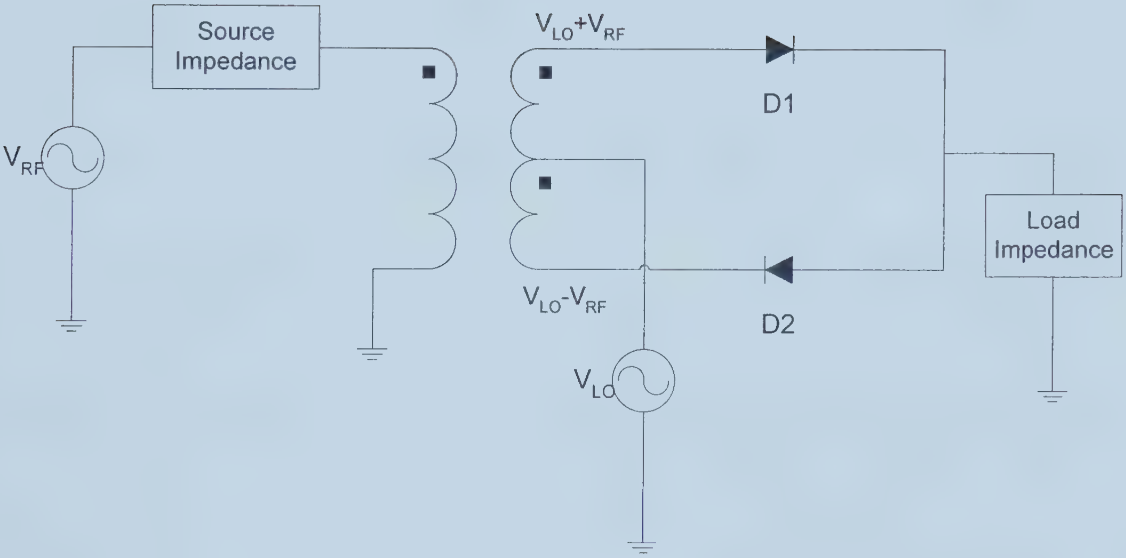


Figure 3-2: Two-Diode Switching Mixer

square wave having the LO frequency. The unit square wave signal can be mathematically represented in as

$$\mathrm{P}_1(t) = \frac{4}{\pi}\sum_{n=0}^{\infty}\frac{\sin[(2n+1)\omega_L t]}{2n+1}. \tag{3.2}$$

Let the amplitude of RF sinusoidal signal be a constant value of $V_{RF.}$ When (3.1) and (3.2) are multiplied and expanded, the result is (3.3). This equation contains the LO signal, the desired frequency translated output signal, and an infinite number of spurious signals of different frequencies created in the mixer. From (3.3), the desired down-conversion term with a conversion gain of 2/π is obtained when n=0 [12]

$$V_{OUT}(t) = V_{LO}(t) + \frac{2V_{RF}}{\pi}\sum_{n=0}^{\infty}\frac{\cos[(2n+1)\omega_L - \omega_{FF}]t - \cos[(2n+1)\omega_L + \omega_{FF}]t}{2n+1}. \tag{3.3}$$

One of the disadvantages regarding the output of two-diode mixer presented in (3.3) is the fact that the $V_{LO}(t)$ is eminently present at the output. In the case where the RF frequency is significantly smaller than the LO frequency, the desired mixing product may be too close to the local frequency, resulting in an impossible or extremely difficult filtering task.

3.1.2 Two-Diode Switching Mixer with Suppressed V_{LO}

One of the disadvantages of the two-diode mixer is the fact that the local oscillator signal is always eminently present at the output. The presence of the LO signal at the output complicates the task of filtering when the LO and RF signals are separated widely in the frequency spectrum.

$$\text{For } \omega_{RF} << \omega_{LO},\ \omega_{IF} = (\omega_{LO} \pm \omega_{RF}) \approx \omega_{LO}. \tag{3.4}$$

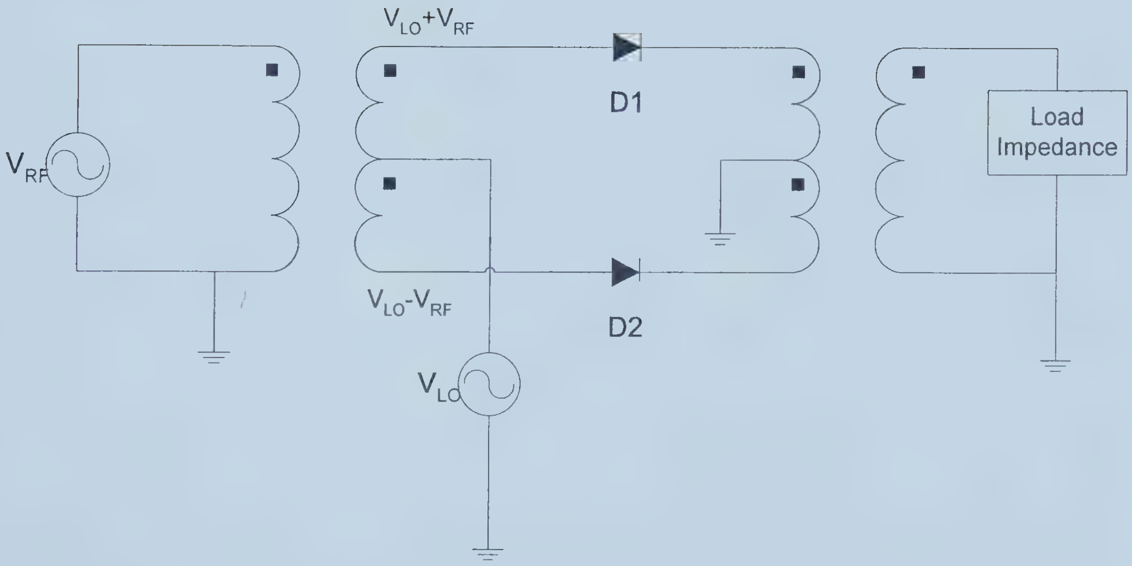


Figure 3-3: Two-Diode Mixer without LO Signal at Output.

Rearrangement of one of the diodes and an introduction of another transformer leads to a switching mixer without presence of LO at the output. The schematic of this switching mixer is shown in Figure 3-3.

Again assuming that the sinusoidal LO signal is significantly larger than the RF signal, the two diodes conduct and switch off at the same time. When the diodes are off, the output will be zero; however when the diodes are conducting, $V_{IF}(t) = V_{RF}(t)$, since the local oscillator currents balance out at the output transformer. (3.5) mathematically represents the operation of the mixer:

$$Vout(t) = V_{RF}(\mathrm{t}) * P_2(t), \quad \text{where } P_2(t) = \begin{array}{l} 1 \text{ when } V_{LO}(t) > 0 \\ 0 \text{ when } V_{LO}(t) < 0 \end{array}. \tag{3.5}$$

The advantage of this switching mixer is that the LO signal is not present at the output. This is apparent when $P_2(t)$ in (3.5) is replaced by its Fourier series shown in (3.6)

$$P_2(t) = \frac{1}{2} + \frac{2}{\pi} \sum_{n=0}^{\infty} \frac{\sin[(2n+1)\omega_L t]}{2n+1}. \tag{3.6}$$

Let $V_{RF}(t)$ be a sinusoidal signal with a constant amplitude of V_{RF}. The resulting output voltage is represented in (3.7). The desired output mixing term has a conversion gain of 1/π and happens when n=0. One can see that there is no V_{LO} component in this signal.

$$\mathrm{V}_{\mathrm{OUT}}(t) = \frac{V_{RF}(t)}{2} + \frac{V_{RF}}{\pi} \sum_{n=0}^{\infty} \frac{\cos[(2n+1)\omega_L - \omega_{FF}]t - \cos[(2n+1)\omega_L + \omega_{FF}]t}{2n+1}. \tag{3.7}$$

3.1.3 Four-Diode Switching Mixer

Using two diodes as switches, two different switching mixers were shown in the previous section. Although the desired frequency translation was achieved in both mixers, the

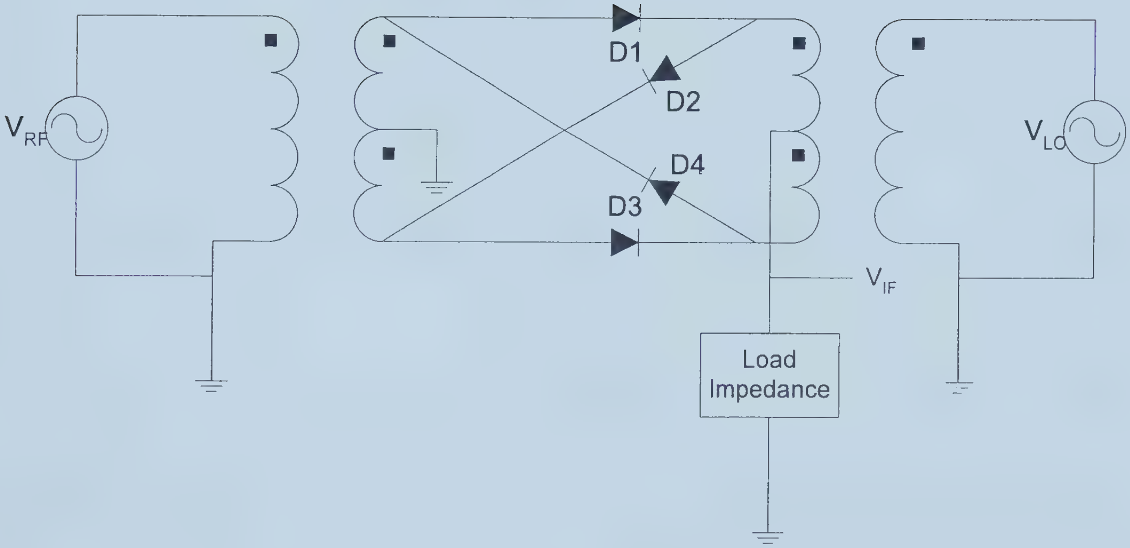


Figure 3-4: Four-Diode Switching Mixer.

presence of local oscillator or radio frequency signals directly at the output can present a difficult filtering task. On the other hand, a switching mixer made up of four diodes with a setup shown in Figure 3-4 does not have LO or RF signals at the output [12]. For the four-diode mixer, when the local oscillator signal is positive, diodes D2 and D3 conduct while diodes D1 and D4 are open. The equivalent circuit for the case when the local oscillator signal is positive is redrawn in Figure 3-5(a). Writing the loop currents for the redrawn circuit in Figure 3-5(a) using Kirchhoff's voltage law, the two loop equations are

$$V_{RF} = (I_1 + I_2)R_{Load} + I_1 R_{diode} - V_{LO}, \tag{3.8}$$

and

$$V_{RF} = (I_1 + I_2)R_{Load} + I_1 R_{diode} + V_{LO}. \tag{3.9}$$

Adding (3.8) and (3.9) and rearranging some terms, the output voltage is as given in (3.10).

$$V_{OUT}(t) = -\frac{V_{RF}(t)R_{LOAD}}{R_{LOAD} + R_{Diode}/2}, \tag{3.10}$$

Similarly, when the local oscillator signal is negative, diodes D1 and D3 conduct while diodes D2 and D3 are open. The equivalent circuit for the case when the local oscillator signal is negative is redrawn in Figure 3-5(b). Using similar steps, the output voltage for the situation when the local oscillator signal is negative is represented in (3.11).

$$V_{OUT}(t) = +\frac{V_{RF}(t)R_{LOAD}}{R_{LOAD} + R_{Diode}/2}. \tag{3.11}$$

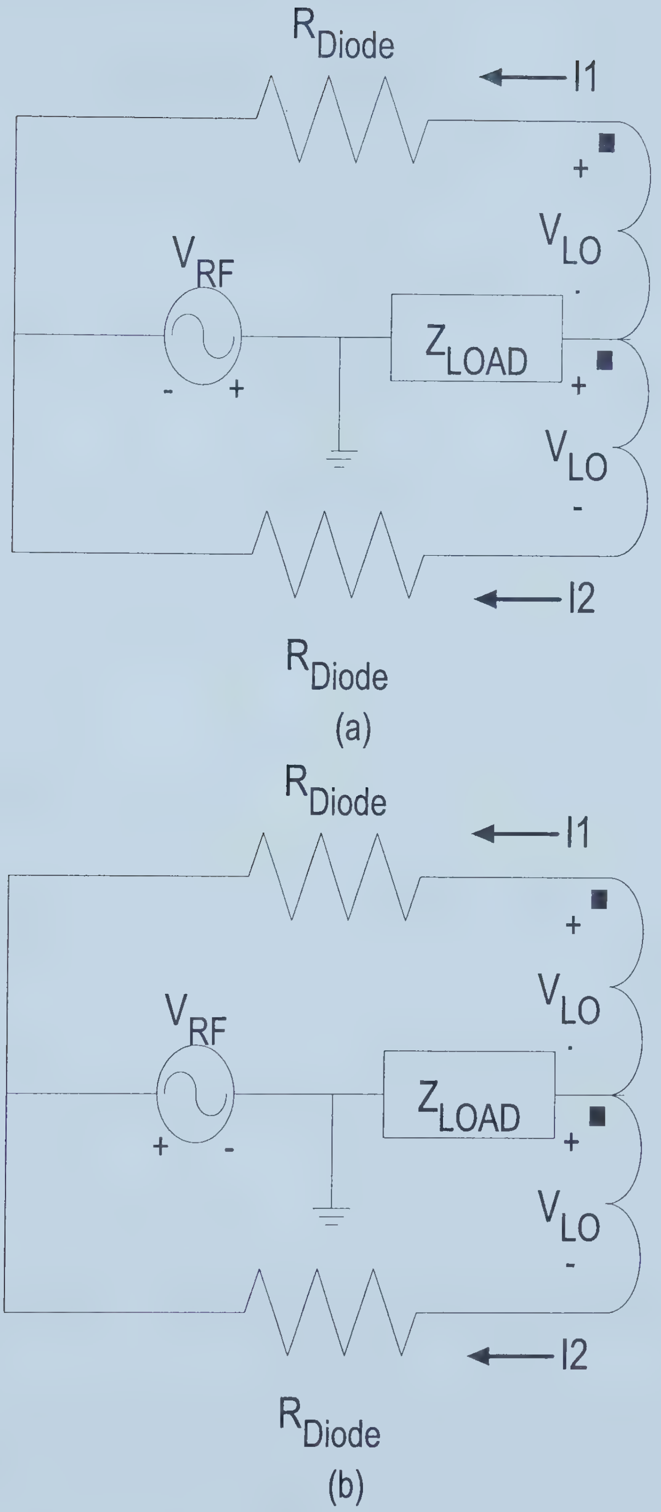


Figure 3-5: Equivalent Four-Diode Switching-Type Mixers.

Combining (3.10) and (3.11) gives (3.12),

$$V_{OUT}(t) = V_{RF}(t) * P_1(t) \frac{R_{LOAD}}{R_{LOAD} + R_{Diode}/2}. \tag{3.12}$$

Substituting the definition for $P_1(t)$ from (3.2) into (3.12) results in (3.13),

$$V_{OUT}(t) = \frac{4V_{RF}R_{LOAD}}{\pi\left(2R_{LOAD} + R_{Diode}\right)}\left(\sum_{n=0}^{\infty} \frac{\cos\left[(2n+1)\omega_{LO} - \omega_{RF}\right]t}{2n+1} - \frac{\cos\left[(2n+1)\omega_{LO} + \omega_{RF}\right]t}{2n+1}\right). \tag{3.13}$$

From (3.13), it is evident that the output voltage is proportional to the input voltage and with the diodes switching at the local oscillator frequency. Assuming the load impedance is significantly larger than diode resistance, the desired mixing term has a conversion gain of $2/\pi$.

3.1.4 Four-MOS Switching Mixer

Inspired by the diode mixer, much research was carried out to create a switching mixer using MOS transistors to facilitate integration [14, 16]. Figure 3-6 shows the core of the MOS switching mixer made up of four n-type MOS transistors. For the setup shown in the schematic, the four transistors operate in pairs connecting the mixer's output port, V_{IF}, to the input port, V_{RF}.

Generally, the sizes of these four transistors used are the same, resulting in the same series resistances in all four transistors. Assume that the series resistance in each of the transistors is the same and denote it by R_{ds}. During the cycle in which the local oscillator signal is positive, transistor pair M1 and M4 connect the input port to the output port while transistor pair M2 and M3 are open.

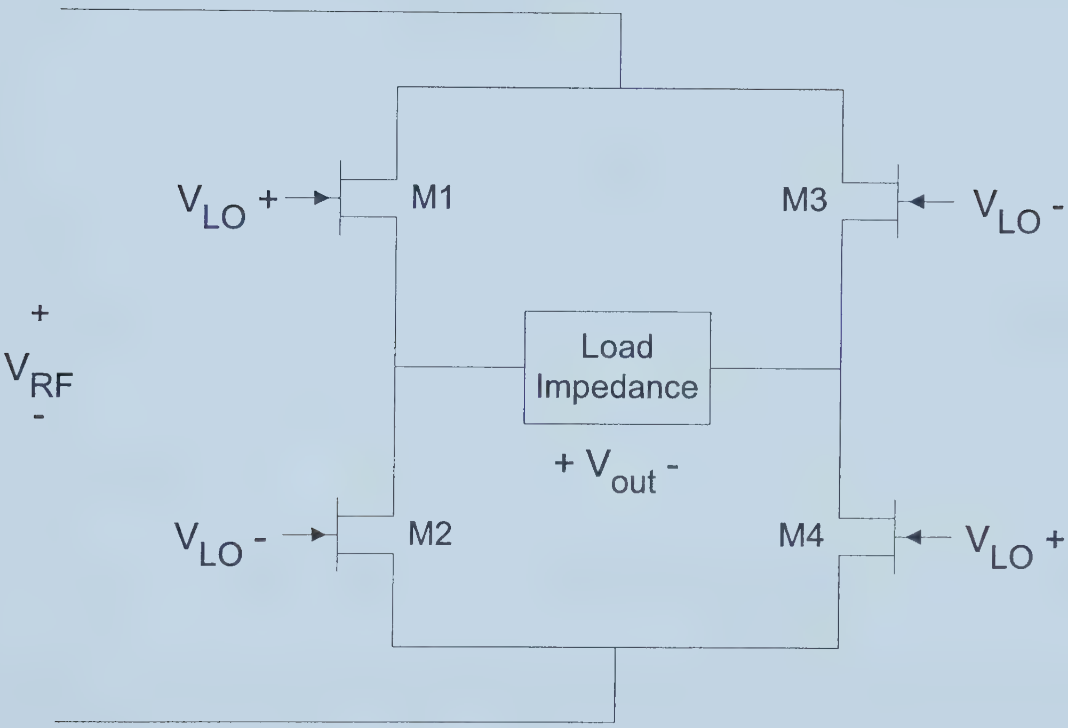


Figure 3-6: CMOS Switching Mixer.

From the redrawn schematic shown in Figure 3-7(a), one can find that the output voltage is

$$V_{OUT}(t) = +V_{RF}(t)\frac{R_{LOAD}}{R_{LOAD} + 2R_{ds} + R_{Source}}. \tag{3.14}$$

During the cycle in which the local oscillator signal is negative, transistor pair M2 and M3 conduct while transistor pair M1 and M4 are open. From the redrawn schematic shown in Figure 3-7(b), one obtains that

$$V_{OUT}(t) = -V_{RF}(t)\frac{R_{LOAD}}{R_{LOAD} + 2R_{ds} + R_{Source}}. \tag{3.15}$$

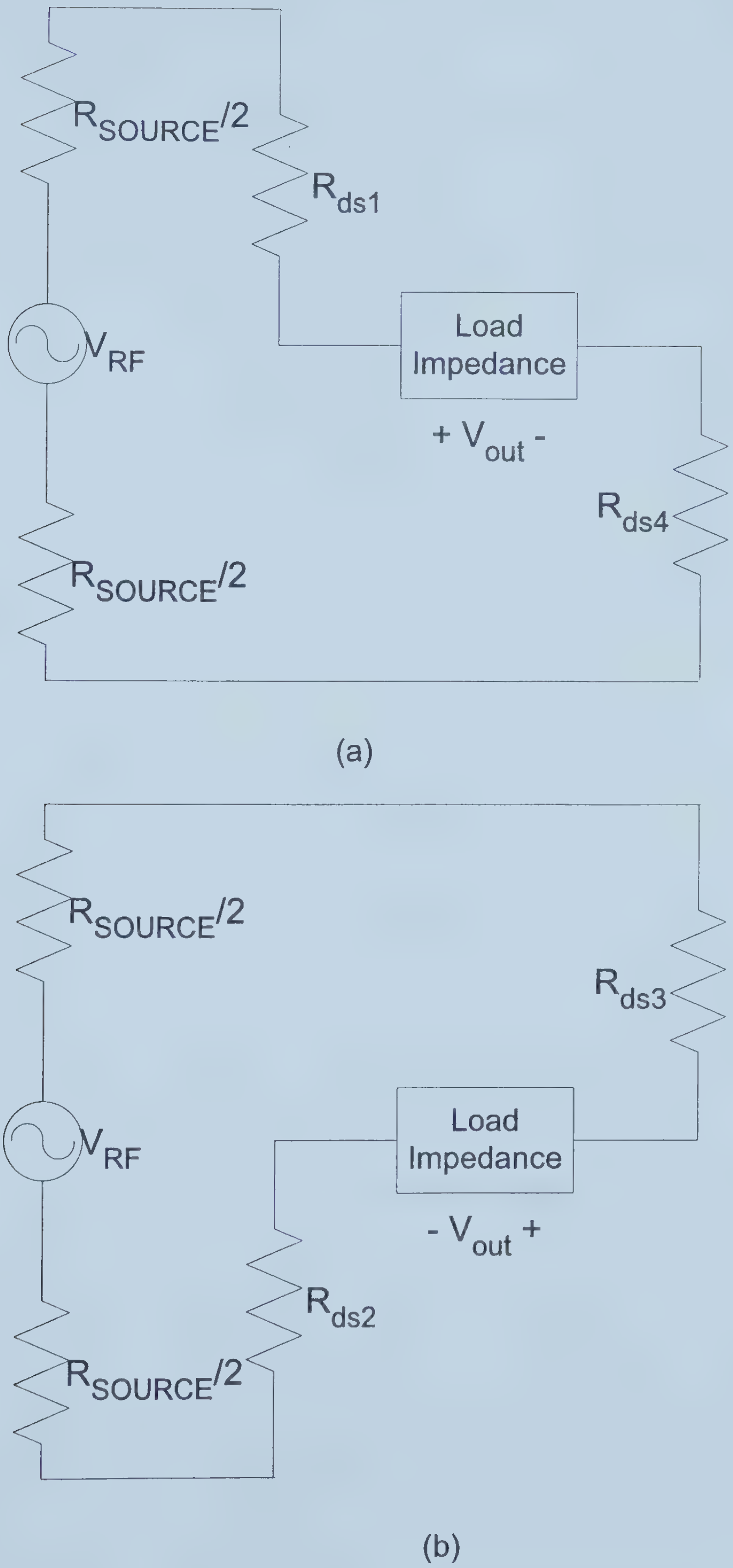
Comparing (3.14) and (3.15), it is evident that the output equations for the two phases differ only in their signs. This is equivalent to the multiplication of the incoming input signal by a unit-amplitude square wave. Consequently, when (3.14) and (3.15) are combined, one has

$$V_{OUT}(t) = V_{RF}(t)\frac{R_{LOAD}}{R_{LOAD} + 2R_{ds} + R_{Source}}P_1(t). \tag{3.16}$$

$P_1(t)$ in (3.16) is a unit-amplitude square wave with local oscillator frequency and is defined by its Fourier series in (3.2). Substituting (3.2) into (3.16) and assuming that the input is a sinusoidal signal with constant amplitude of V_{RF}, we obtain that

$$V_{OUT}(t) = \frac{2V_{RF}R_{LOAD}}{\pi(R_{LOAD} + 2R_{ds} + R_{Source})}\begin{bmatrix} \cos(\omega_{LO} - \omega_{RF})t + \\ \cos(\omega_{LO} + \omega_{RF})t + \ldots \end{bmatrix}. \tag{3.17}$$

The first two terms showing the desired mixing term and the image component are shown in (3.17) with the rest of the harmonic terms left out. The conversion gain obtained using four CMOS switches is 2/π, assuming that the series resistance of transistors and source resistance are significantly smaller than the load resistance.



(a)

(b)

Figure 3-7: Redrawn CMOS Switching Mixer in Each Phase of LO Signal.

3.2 Multiplying Mixer

From Section 3.1, switching mixers provide the desired frequency conversion but the need to achieve the desired gain with acceptable compromise in gain, speed, linearity, and noise makes the use of switching mixers undesirable in the some situations. As an alternative architecture, multiplying mixers operate based on the square law principle. A demonstration of the principle of operation for multiplication-based frequency mixers is illustrated in Figure 3-8. In the figure, an input sinusoidal signal of frequency 90MHz is multiplied by the mixing function, also a sinusoidal signal, of frequency 100MHz. The output produced contains two frequency components, the sum and the difference of the input and mixing function.

Mixers based on multiplication may achieve high conversion gain, unlike the switching mixers that can only achieve no more than unity in power conversion gain [17]. Many of the mixer modules used provide frequency translation but with conversion loss. By using a mixer module with a conversion gain instead of a loss, it is possible to reduce the number of amplification blocks in a system. This reduction helps in reducing power consumption and noise while still maintaining the desired overall gain.

Multiplying mixers use the square-law characteristics that are often associated with bipolar and CMOS technologies. Often, both the input RF signal and the LO signal are applied to the transistors such that they add to the bias voltage. The total voltage is applied to the transistors and is converted into current, taking advantage of the device's square-law behavior to create the mixing effects.

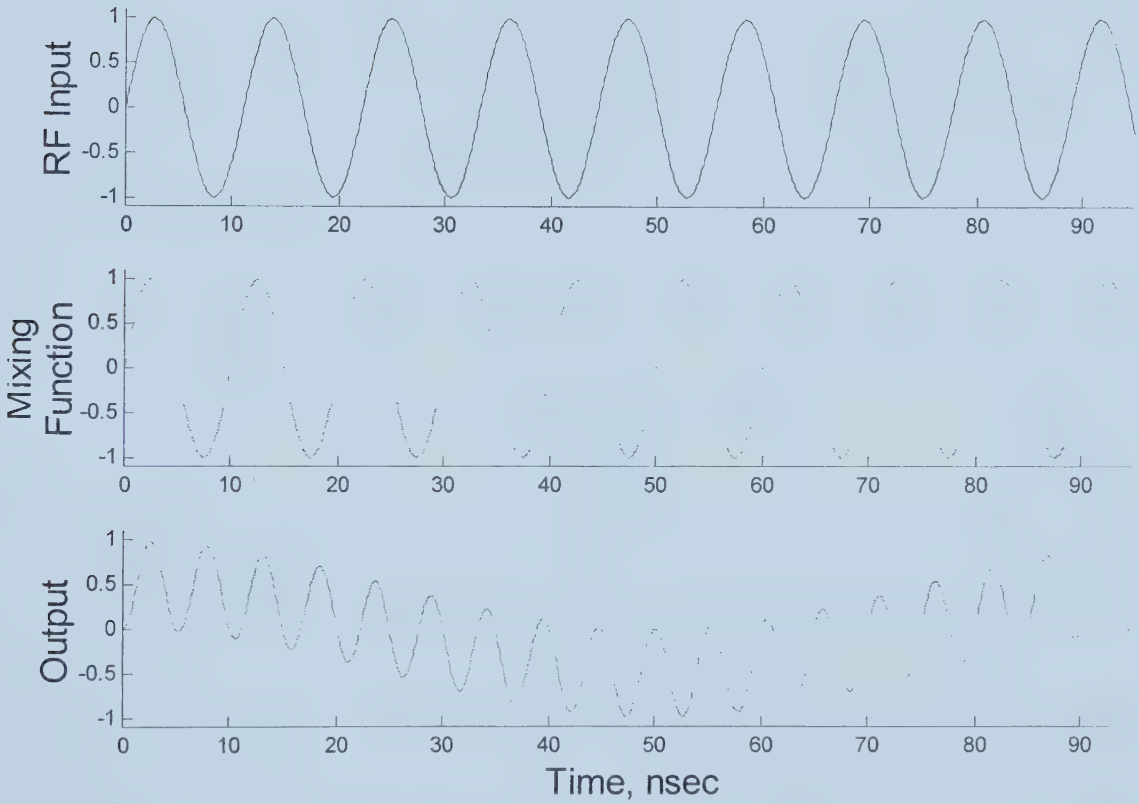


Figure 3-8: Principle of Operation of Multiplying Mixer in Time Domain.

This section will detail schematics and principle of operation for multiplying mixers based on common-source and differential pair configuration.

3.2.1 Single Device CMOS Square-Law Mixer

When complementary metal-oxide-semiconductor field-effect (MOS) transistors are switched on and conducting, the transistors will be operating in triode or saturation (constant-current) regions. The current flowing from the drain terminal to the source terminal when an n-type MOS transistor is biased in the triode and active regions is described by the following equations

$$I_{DS} = \mu C_{OX}\frac{W}{L}\left[(V_{GS}-V_T)V_{DS}-\frac{V_{DS}^2}{2}\right]^2, \tag{3.18}$$

$$I_{DS} = \frac{\mu C_{OX}}{2}\frac{W}{L}(V_{GS}-V_T)^2. \tag{3.19}$$

In both instances, the drain-source current includes a term proportional to the square of voltage; this square-law property makes the MOS transistor a candidate to be part of a frequency mixer.

Although MOS transistors exhibit the square-law property when the transistor conducts and operates in both triode and constant current regions, the application for frequency mixing when the transistor is biased in the triode region is quite complex. The dependency of drain-source current on the drain-source voltage when the transistor is operating in the triode region limits its usefulness in mixing. However, when the transistor is operating in the constant current region, the drain-source current is proportional to the square of the difference between the gate-source and threshold voltages. Assuming that the gate-source voltage is a linear combination of two sinusoidal

voltage signals, the drain-source current will contains a term that is the product of these two sinusoidal voltage signals. When the square-term is expanded, it will show the required frequency conversion.

One of the simplest configurations to harness the square-law property is derived from the classic single-stage common-source amplifier [12, 17]. In Figure 3-9, the transistor M1 is biased to operate in the constant current region via a bias network. The radio frequency signal is applied to the gate terminal, whereas the local oscillator signal is connected to the gate terminal through a DC blocking capacitor. Let V_{DC} be the gate-source bias voltage and assume the input radio frequency and the local oscillator signals are both sinusoidal with constant amplitudes of V_{RF} and V_{LO} respectively. The total drain-source current flowing through M1 is given in (3.20),

$$I_{DS,\text{Total}} = \frac{\mu C_{OX}}{2}\frac{W}{L}\left(V_{DC} + V_{RF}\cos\omega_{RF}t + V_{LO}\cos\omega_{LO}t - V_T\right)^2. \tag{3.20}$$

The total output current obtained by expanding (3.20) is

$$I_{DS,\text{Total}} = \frac{\mu C_{OX}}{2}\frac{W}{L}\begin{bmatrix}\left(V_{DC} - V_T\right)\left(V_{DC} - V_T + 2V_{RF}\cos\omega_{RF}t + 2V_{LO}\cos\omega_{LO}t\right)\\ +V_{RF}^2\cos^2\omega_{RF}t + V_{LO}^2\cos^2\omega_{LO}t\\ +2V_{RF}V_{LO}\cos\omega_{RF}t\cos\omega_{LO}t\end{bmatrix}. \tag{3.21}$$

The last term in (3.21) is clearly showing a multiplication between two sinusoidal voltage signals, producing the mixing signal and its image in the current domain.

Mixers using the common-source configuration setup obtain frequency mixing by first converting the voltage into a current. Employing the square-law property of MOS transistors, both the radio frequency and local oscillator voltage signals are multiplied together to yield the desired frequency term with a transconductance conversion gain of $\mu C_{OX}V_{LO}W/L$.

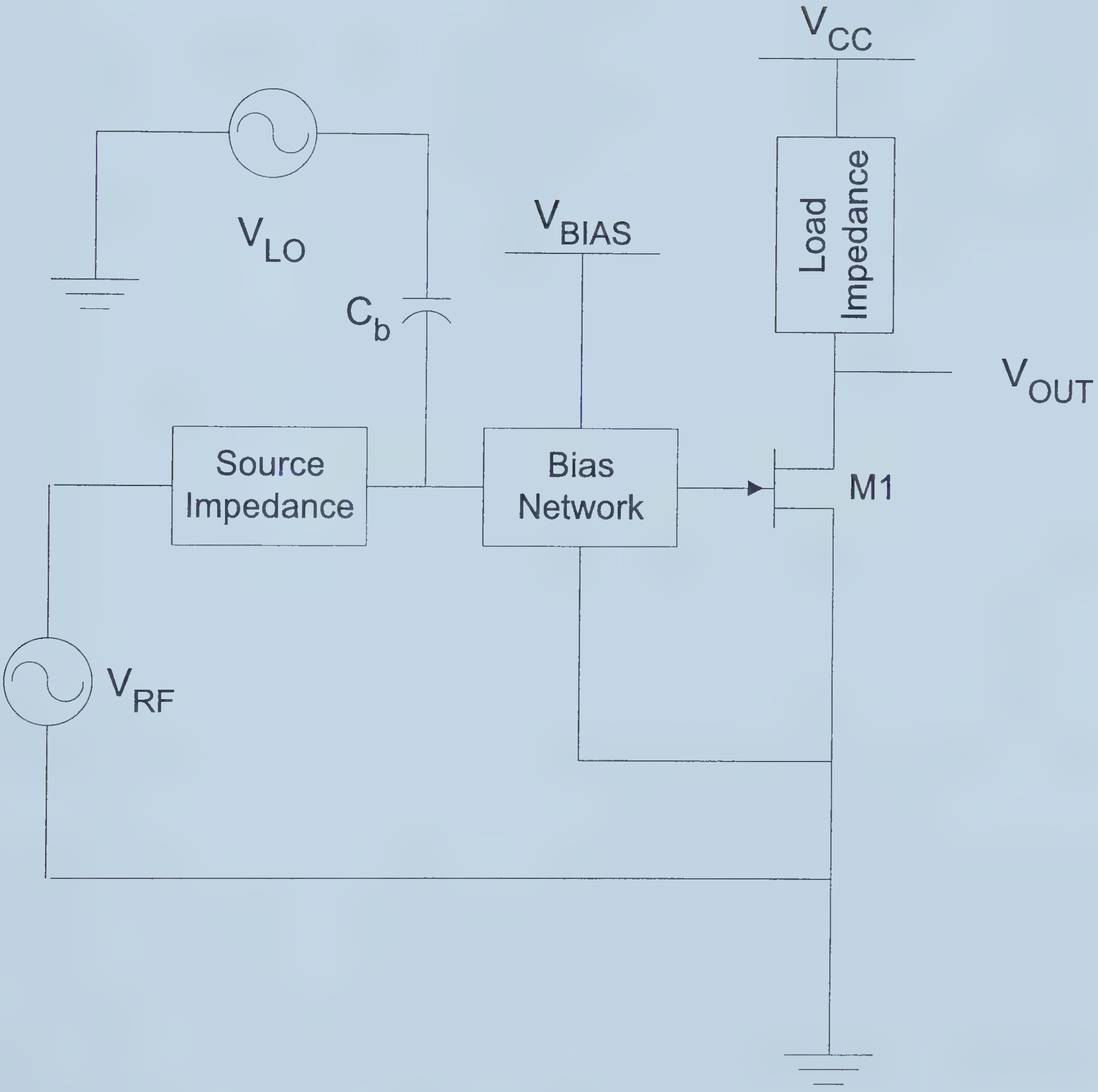


Figure 3-9: A Square-Law Mixer Using Single CMOS Device.

Often the output current is converted back into the voltage domain using a load impedance implemented by a MOS transistor acting as a resistor or inductor-capacitor circuit that is tuned to the desired IF frequency.

3.2.2 Single-Balanced Mixer

Single MOS transistor mixers generate the desired mixing. However, along with the desired frequency translated output, numerous other signals are also generated by the square-law property. Among the generated signals there are two signals containing frequency components of the radio frequency and local oscillator frequency. In situations where the difference in frequency spectrum between the input signal and the local oscillator is large, the desired mixing term can be difficult to extract.

Inspired by the possibility of providing conversion gain using the common-source amplifier and performing frequency mixing in the current domain, a new design was invented based on a combination of a differential pair and common-source configuration resulting in the creation of a single-balanced mixer [12]. The schematic of the single-balanced mixer is presented in Figure 3-10, showing three transistors that form the basic core of operation. Bias current for all three transistors is provided by biasing of transistor M1 via a bias network. The input radio frequency signal is applied to the gate terminal of transistor M1, whereas the local oscillator signal and its counter phase are applied to the gate of the differential transistor pair M2 and M3.

Transistor M1 converts the input RF voltage signal into current forming the total tail current, which consists of the bias current and a sinusoidal current signal whose frequency is that of the radio frequency.

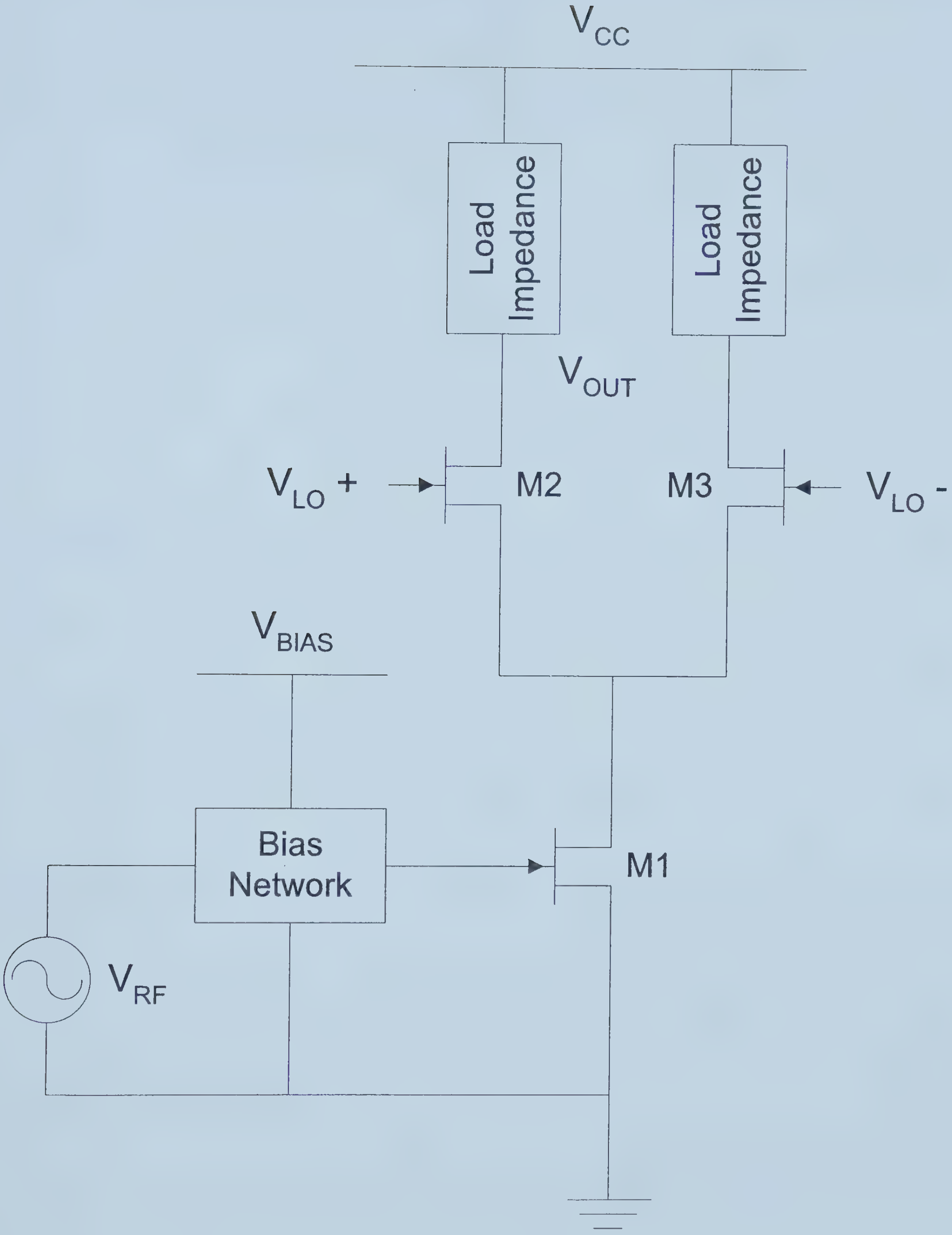


Figure 3-10: Basic Schematic of Single-Balanced Mixer.

Generally, the transistors of differential pair M2 and M3 are of the same size and are biased the same way. This feature results in equal bias currents for both transistors, leading to the same transconductance for M2 and M3, $g_{m2} = g_{m3}$. As the differential pair transistors has equal bias currents and transconductances, the small signal currents for M2 and M3 are

$$i_{d2}(t) = +g_m \frac{V_{LO}(t)}{2}, \tag{3.22}$$

and

$$i_{d3}(t) = -g_m \frac{V_{LO}(t)}{2}. \tag{3.23}$$

Increasing the circuit immunity to environmental noise, differential output is taken over single-end output [11-12] by defining the differential output

$$i_{out}(t) = i_{d2}(t) - i_{d3}(t) = g_m V_{LO}(t). \tag{3.24}$$

as the difference between (3.22) and (3.23).

$$g_m = \sqrt{\mu C_{OX}\left(W/L\right) I_{DS}}. \tag{3.25}$$

Then substituting the definition for transconductance from (3.25) into (3.24), along with the approximation of I_{Bias} being significantly larger than the small signal component in

$$i_{out}(t) = V_{LO}(t)\sqrt{\mu C_{OX}\left(W/L\right)}\sqrt{I_{Bias} + I_{RF}\cos\omega_{RF}t}. \tag{3.26}$$

that can be approximated as

$$i_{out}(t) \approx \sqrt{\mu C_{OX}\left(W/L\right) I_{Bias}}\left(1 + \frac{I_{RF}\cos\omega_{RF}t}{2I_{Bias}}\right) V_{LO}(t). \tag{3.27}$$

The local oscillator signal level is chosen large enough to ensure that transistor M2 and M3 alternately switch all the tail current from one side to the other side of the differential

pair. This switching of tail current generates a unit square wave whose frequency is that of the local oscillator. Substituting the Fourier series for a unit square wave for $V_{LO}(t)$ in (3.27) results in,

$$i_{out} \approx \sqrt{\mu C_{OX}\left(W/L\right) I_{Bias}}\left(1 + \frac{I_{RF}\cos\omega_{RFz}t}{2I_{Bias}}\right)\frac{4}{\pi}\left[\cos\omega_{LO}t + \frac{1}{3}\cos 3\omega_{LO}t + \ldots\right]. \quad (3.28)$$

By expanding (3.28) multiplication between two sinusoidal signals produces frequency shifts that are clearly seen in (3.29), along with the absence of any signals having radio frequency signal components.

$$i_{out} \approx \frac{4}{\pi}\sqrt{\mu C_{OX}\left(W/L\right) I_{Bias}}\begin{pmatrix}\left[\cos\omega_{LO}t + \frac{1}{3}\cos 3\omega_{LO}t + \ldots\right] + \frac{I_{RF}\cos\omega_{RF}t\cos 3\omega_{LO}t}{6I_{Bias}} \\ \frac{I_{RF}}{4I_{Bias}}\left[\cos\left(\omega_{RFz} - \omega_{LO}\right)t + \cos\left(\omega_{RFz} + \omega_{LO}\right)t\right] + \ldots\end{pmatrix}. \quad (3.29)$$

Single-balanced mixers employ two different common analog amplification stages to achieve frequency conversion. Input radio frequency voltage is first converted into current. After conversion, the current signal is multiplied by a unit square wave to produce the desired frequency conversion. The conversion gain obtained using the single-balanced mixer is

$$G = \frac{I_{RF}Z_L}{\pi\sqrt{I_{Bias}}}\sqrt{\mu C_{OX}\left(W/L\right)}, \quad (3.30)$$

and often the differential output is converted back into the voltage domain to be used in subsequent modules along the signal path.

3.2.3 Fully-Balanced (Quad) Mixer

Encouraged by the success in eliminating signals with frequency components from the output by using differential pairs, this concept is once again employed to create the fully

balanced mixer, commonly known as the Gilbert Multiplier Cell. B. Gilbert first designed this analog multiplier cell in 1968. This design methodology has become a popular choice for analog multiplication and frequency mixing due to its superior harmonic removal and better noise figure [12, 17-19].

Using two single-balanced mixers to produce the quad mixer, one obtains the schematic shown in Figure 3-11. Six transistors make up the core of the mixer. Transistors M1 and M2 are connected in the common-source configuration while the other four transistors form the two crisscrossed differential pairs. Transistors M1 and M2 are used as voltage-to-current converters for the input radio frequency voltage signal and its counter phase. With sufficiently large local oscillator signal level, the differential pairs switch the tail current from one side of the differential pair to the other and generate two counterphase square waves having a frequency equal to that of the local oscillator.

With changes in the polarity of the local oscillator, the output current taken differentially is

$$i_{OUT}(t) = i_{OUT1}(t) - i_{OUT2}(t) = i_A(t) - i_B(t)\,, \tag{3.31}$$

when the local oscillator is positive, and

$$i_{OUT}(t) = i_{OUT1}(t) - i_{OUT2}(t) = i_B(t) - i_A(t)\,. \tag{3.32}$$

when the local oscillator is negative.

By combining (3.31) and (3.32), one obtains the output

$$i_{OUT}(t) = \left(i_A(t) - i_B(t)\right)\frac{4}{\pi}\left[\cos\omega_{LO}t + \frac{1}{3}\cos 3\omega_{LO}t + \frac{1}{5}\cos 5\omega_{LO}t + \ldots\right]. \tag{3.33}$$

where the unit square wave expressed in its Fourier series,

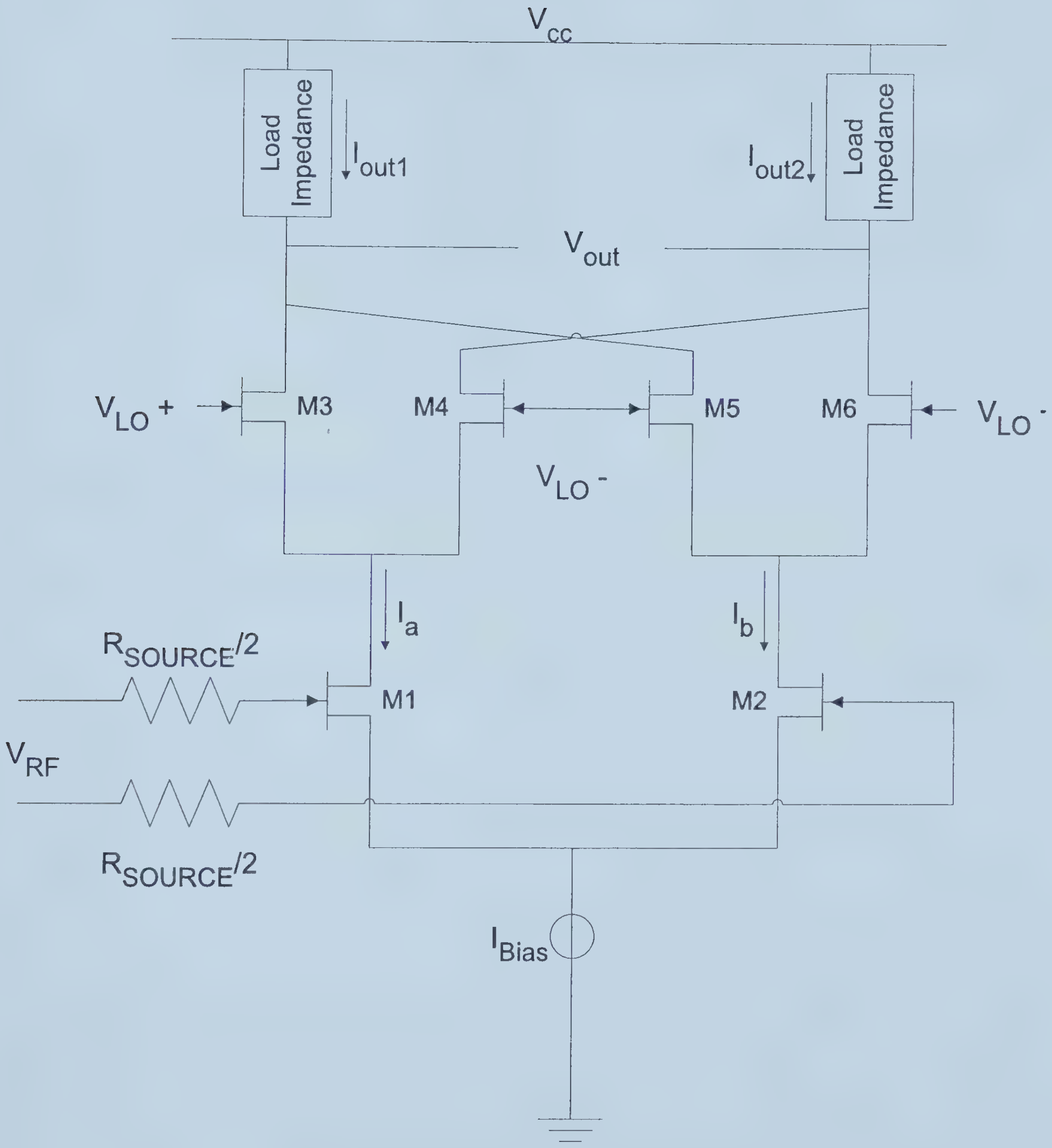


Figure 3-11: Basic Schematic of Fully Balanced Mixer.

With transistor M1 and M2 operating in the saturation region, i_A and i_B are expressed as

$$i_A(t) = \frac{1}{2}\mu C_{OX}\frac{W_1}{L_1}\left(V_{DC} + V_{RF}^{+}(t) - V_T\right)^2, \tag{3.34}$$

$$i_B(t) = \frac{1}{2}\mu C_{OX}\frac{W_2}{L_2}\left(V_{DC} + V_{RF}^{-}(t) - V_T\right)^2. \tag{3.35}$$

Assuming that both transistors M1 and M2 have the same width and length, the difference between the currents (*$i_A(t)$* and *$i_B(t)$*) after computation and simplification is shown is

$$i_A(t) - i_B(t) = \mu C_{OX}\frac{W_1}{L_1}\left(V_{DC} - V_T\right)V_{RF}(t). \tag{3.36}$$

This equation is substituted into (3.33) to yield

$$i_{OUT}(t) = \frac{4}{\pi}\mu C_{OX}\frac{W_1}{L_1}\left(V_{DC} - V_T\right)V_{RF}(t)\left[\cos\omega_{LO}t + \frac{1}{3}\cos 3\omega_{LO}t + \frac{1}{5}\cos 5\omega_{LO}t + \ldots\right]. \tag{3.37}$$

Assuming that the input radio frequency signal is $V_{RF}sin\omega_{RF}(t)$. When this signal is substituted into (3.37), one obtains

$$i_{OUT}(t) = \frac{4}{\pi}\mu C_{OX}\frac{W_1}{L_1}\left(V_{DC} - V_T\right)V_{RF}\begin{bmatrix}\frac{1}{2}\cos(\omega_{RF} - \omega_{LO})t + \frac{1}{2}\cos(\omega_{RF} + \omega_{LO})t + \\ \frac{1}{6}\cos(\omega_{RF} - 3\omega_{LO})t + \frac{1}{6}\cos(\omega_{RF} + 3\omega_{LO})t + \ldots\end{bmatrix}. \tag{3.38}$$

From (3.38), the frequency converted terms are clearly observed. Signals with input radio frequency and local oscillator frequency are absent at the output while all unwanted even order harmonics at the output are canceled. Conversion gain obtained using the Gilbert multiplier cell design is

$$G = \frac{2\mu C_{OX}}{\pi}\frac{W_1}{L_1}\left(V_{DC} - V_T\right)Z_L. \tag{3.39}$$

and it is dependent on the ratio of the transistors used.

3.3 Enhancements to the Multiplying Mixer

Two modifications are often made to the multiplier-based mixers for better performance—additional linearization and zero-headroom AC current source.

3.3.1 Additional Linearization Modification

Imperfections of realistic frequency mixers often generate additional harmonic spurious responses and decrease the linearity. One technique used to maximize the linearity of multiplier mixers is based on the commonly used degenerated common source CMOS amplifier stage. Figure 3-12 shows a schematic of an n-type CMOS transistor in a common source setup with addition of an impedance between the source terminal and the ground. The square-law property of the transistor depends on the overdrive voltage that can introduce excessive nonlinearity; the use of the degeneration impedance will reduce this nonlinearity effect and increases the dynamic range [20].

The introduction of the degenerated impedance leads to a smoother variation of the drain-source current, giving the common-source stage a transconductance that can be approximated as,

$$\text{Transconductance} \approx \frac{1}{\text{Degeneration impedance}}. \tag{3.40}$$

At low frequency, resistors are often used as the degenerated impedance. At high frequency, the use of inductors offers several advantages such as the absence of thermal noise or DC voltage drop. The increasing reactance of an inductor with the increasing frequency also helps to attenuate high frequency harmonic and intermodulation components [17]. This process of linearization can be used on the common-source, single-balanced or the fully balanced mixers.

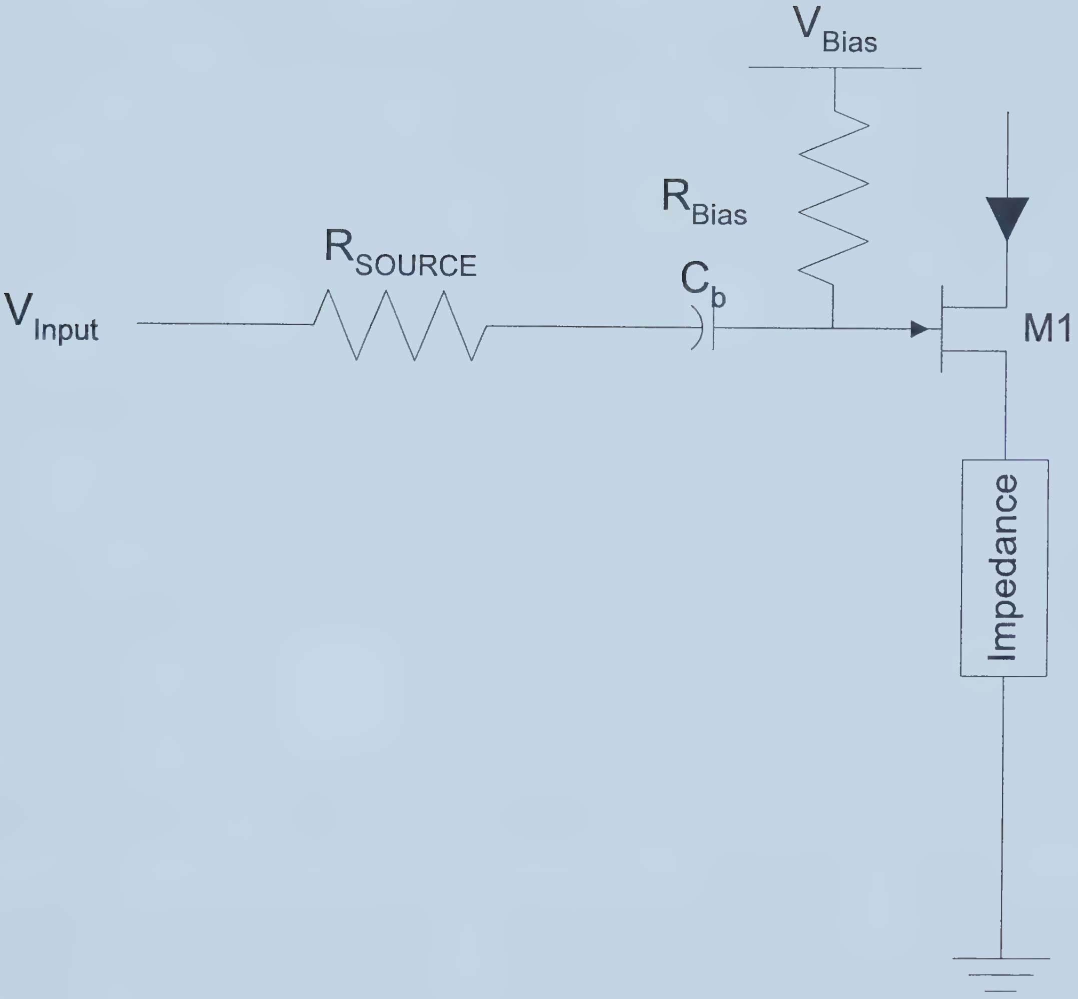


Figure 3-12: Linearization Based on Source-Degeneration.

3.3.2 Minimum Supply-Headroom Modification

Development in CMOS technology resulted in a decrease in the shortest effective length of transistors, and along with this decrease in effective length, the maximum allowed supply voltage had also been reduced to prevent any static charge damage. This reduction in the maximum allowed supply voltage leads to a lack of voltage headroom for voltage swing. Figure 3-13 shows an ideal current source that is used to provide bias for transistors. The commonly used method in place of the ideal current source is the implementation of transistors or resistors to provide the necessary current. However, the use of transistors or resistors to supply the bias current consumes voltage headroom. An inductor-capacitor tank can be used in place of the ideal current source creating a zero-headroom AC current source. When used to supply bias current for a differential pair, the resonant frequency of the tank is selected to reject the most objectionable common-mode components.

3.4 Examples of Mixers in Literature

3.4.1 Switching Frequency Mixer in Literature

With the achievable conversion gain fixed at $2/\pi$, not a lot of work was carried out to determine the performances of frequency mixers that base their principle of operation on switching. One such work dedicated to switching frequency mixers was [16]. 0.5μm CMOS technology was chosen in the implementation and experimentation. The performance metrics are listed in Table 3-1.

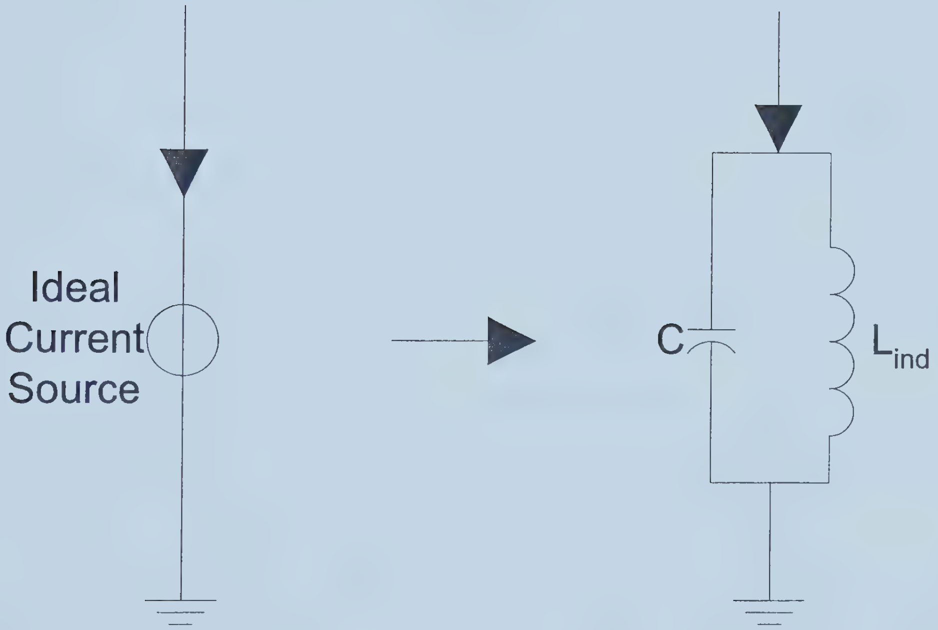


Figure 3-13: Zero-Headroom Current Source.

Power	≤500μW
Voltage Conversion Gain (dB)	-7.3
Noise Figure (dB)	6
Input-IP3 (dBm)	4
Technology	0.5μm CMOS
Die Area (exclude pads) (mm^2)	0.0084

Table 3-1: Switching Frequency Mixer Performance.

3.4.2 Multiplying Frequency Mixer in Literature

One of the most popular designs is based on the Gilbert multiplier cell. Numerous works carried out in different technologies such as Silicon Bipolar, Gallium Arsenide, and CMOS can be readily found in the literature. From the works found in [18-19, 21-24], multiplying frequency mixers having a similar architecture to the CMOS fully balanced frequency mixer have been fabricated in Silicon Bipolar technology. The typical performances of these frequency mixers are summarized in Table 3-2.

Power	2.82mW
Voltage Conversion Gain (dB)	-2.5
Noise Figure (dB)	11.89
Input-IP3 (dBm)	15.75
Technology	Silicon Bipolar
Die Area (mm^2)	2.04

Table 3-2: Silicon Bipolar Multiplying Frequency Mixer Performance.

Of the most popular technologies used is CMOS technology, most of the works found in the literature are often associated with integration of baseband circuitry. Literature [25-35] highlight some of the works done that revolves around CMOS Gilbert multiplier cells

design. Typical performances of a CMOS fully balanced frequency mixer are summarized in Table 3-3.

Power	17mW
Voltage Conversion Gain (dB)	0
Noise Figure (dB)	24
Input-IP3 (dBm)	21
Technology	0.8μm-0.35μm CMOS
Die Area (excluding pad) (mm^2)	0.0036 (0.8μm CMOS)

Table 3-3: Typical CMOS Multiplying Frequency Mixer Performance.

Chapter 4

4.0 Basis for Experimental Mixers

In consideration of higher gain and linearity requirements for new cellular telephony and the lowering of the maximum allowed power supply for CMOS technology, experiments were carried out to determine the feasibility of implementing frequency mixers using 0.18µm CMOS technology for 3G wireless communication. Using two performance metrics—Gain and Third-Order Intercept point—as a guide, one frequency mixer based on the switching and another based on the multiplication principle of operation were designed, fabricated, and tested. Both mixers were designed with the intention of implementation in the receiver path while meeting the standardized requirements for 3G W-CDMA cellular systems. Table 4-1 shows the necessary requirements imposed on LNA and mixers for the new cellular systems available from [36]. The table shows that a frequency mixer must have a minimum of 10dB gain and a minimum of 10dBm in input third-order intercept point characteristic for 3G W-CDMA.

	LNA	Mixer
Gain (dB)	15±1	10±1
Selectivity (dB)	≥0	≥0
Noise Figure (dB)	≤2.5	≤15
Input-IP3 (dBm)	≥-3	≥10

Table 4-1: Block Specification for 3D W-CDMA for LNA and Mixer.

4.1 Experimental Simulation Design

4.1.1 Switching Mixer

A design chosen was based on [14]. It consists of a of four CMOS transistor switching mixer, and a filter network connected to the input ports. N-type enhancement transistors with a width of 90µm and a length 0.6µm were drawn to avoid short-channel operation. Numerical values for the passive devices that formed the filter network were first calculated and matched in the computer simulation.

Inductors used in the filter network were on-chip inductors created by routing the highest layer of metal around in a square orientation such as that shown in Figure 4-1. Using (4.1) and (4.2) from [37], the area of the spiral inductors was determined. With a pitch of 0.2turns/µm, the number of turns needed was first determined for a desired inductor value using (4.1). The dimension of the inductor was then determined using (4.2). In hope of obtaining reasonable sizes, two values of inductors, 5nH and 10nH, were chosen. Using (4.1) and (4.2), it was determined that the 5nH inductor has 10 turns and a width of 83.4µm and the 10nH inductor should have 12 turns and a width of 115.6µm.

$$n \approx \left[\frac{PL_{IND}}{1.2*10^{-6}}\right]^{1/3}. \tag{4.1}$$

$$L_{IND} \approx 1.2*10^{-6} n^2 r. \tag{4.2}$$

The schematic of the experimental switching mixer consisting of the transistors and the filter network is given in Figure 4-2. The filter network created using the on-chip passive devices tuned to the 3 GHz. The analysis is broken into two parts, inductors and capacitors connected in series, and inductors and capacitors connected in parallel.

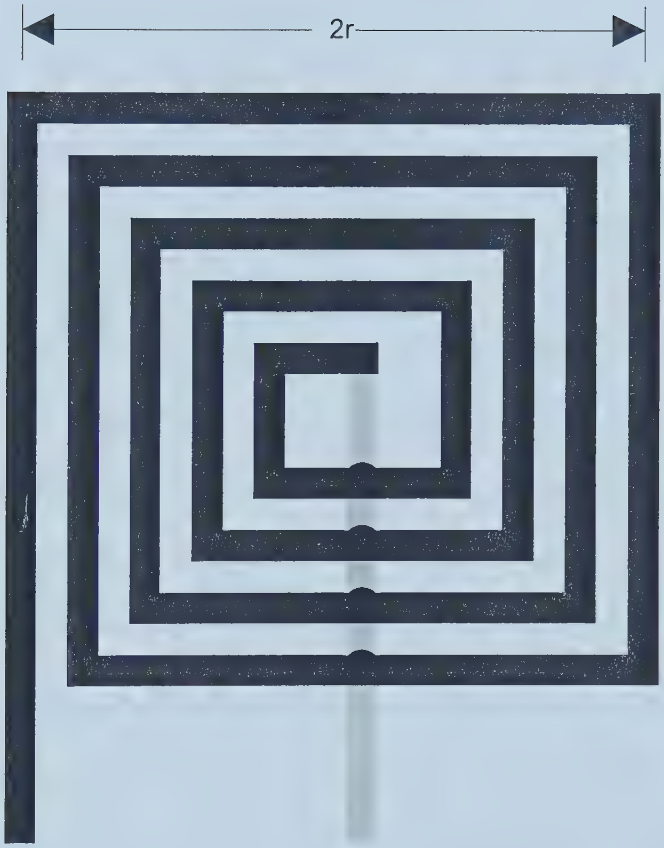


Figure 4-1: Spiral On-Chip Inductor.

Two sets of series arrangements of an inductor and a capacitor form LC circuits that create a short-circuit at the tuned frequency with the resonant frequency define by

$$\omega_{RES} = 1 \Big/ \sqrt{L_{ind,1} C_1} \, . \tag{4.3}$$

Using (4.3) and a series inductor of 10nH in value, the value of the series capacitor was determined to be 281.4fF for a tuned frequency of 3 GHz.

An open-circuit at the tuned frequency is desired for the parallel arrangement of an inductor and a capacitor. Letting L_3 and L_4 be the same and equal to 5nH, capacitor C_3 was determined to be 281.4fF using (4.4) for the tuned frequency of 3 GHz.

$$\omega_{RES} = \omega_{RF} = 1 \Big/ \sqrt{\left(L_{ind,3} + L_{ind,4}\right) C_3} \, . \tag{4.4}$$

On-chip capacitors were created by placing two metal plates on top of each other, and as a precautionary step, a resistor R_1 was placed between ground and the inductors L_3 and L_4. The resistor R_1 had a value of 50 Ω and used to prevent any short-circuit to ground at frequencies away from the tuned frequency. Figure 4-2 shows the schematics of the switching mixer with the actual values for all passive devices used. Unfortunately, due to the effect of lateral flux, the fabricated capacitors had a value of 283.1fF instead of the desired values. The difference in the capacitor values resulted in a tuned frequency of 2.991 GHz with a 0.3% deviation from the desired frequency.

The designed voltage conversion gain for this experimental switching frequency mixer with both R_{LOAD} and R_{Source} having the value of 50Ω is

$$G \approx \frac{2R_{LOAD}}{\pi\left(R_{LOAD} + R_{Source}\right)} \, . \tag{4.5}$$

and is equal to -10dB.

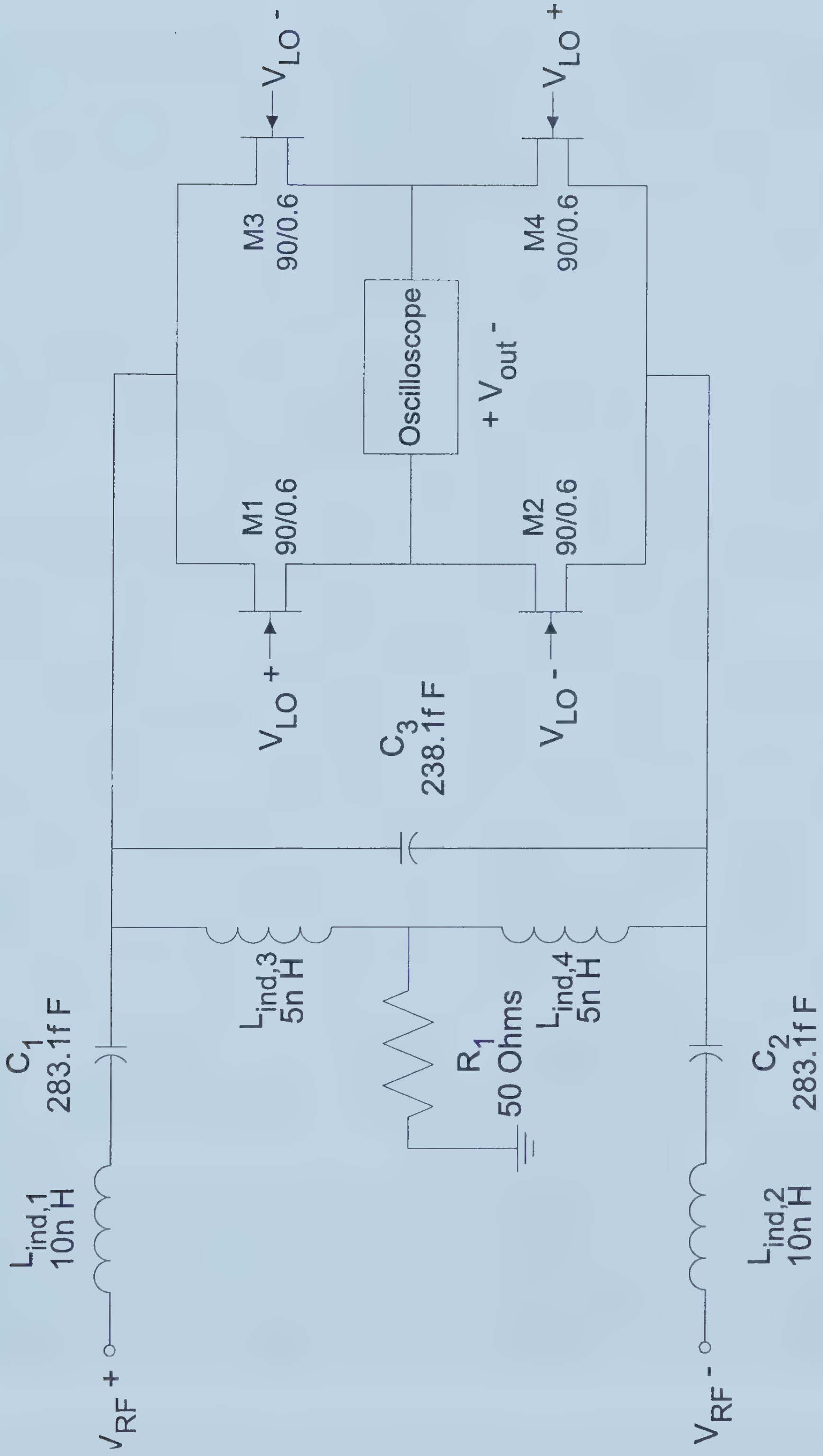


Figure 4-2: Schematic of Experimental Switching Mixer.

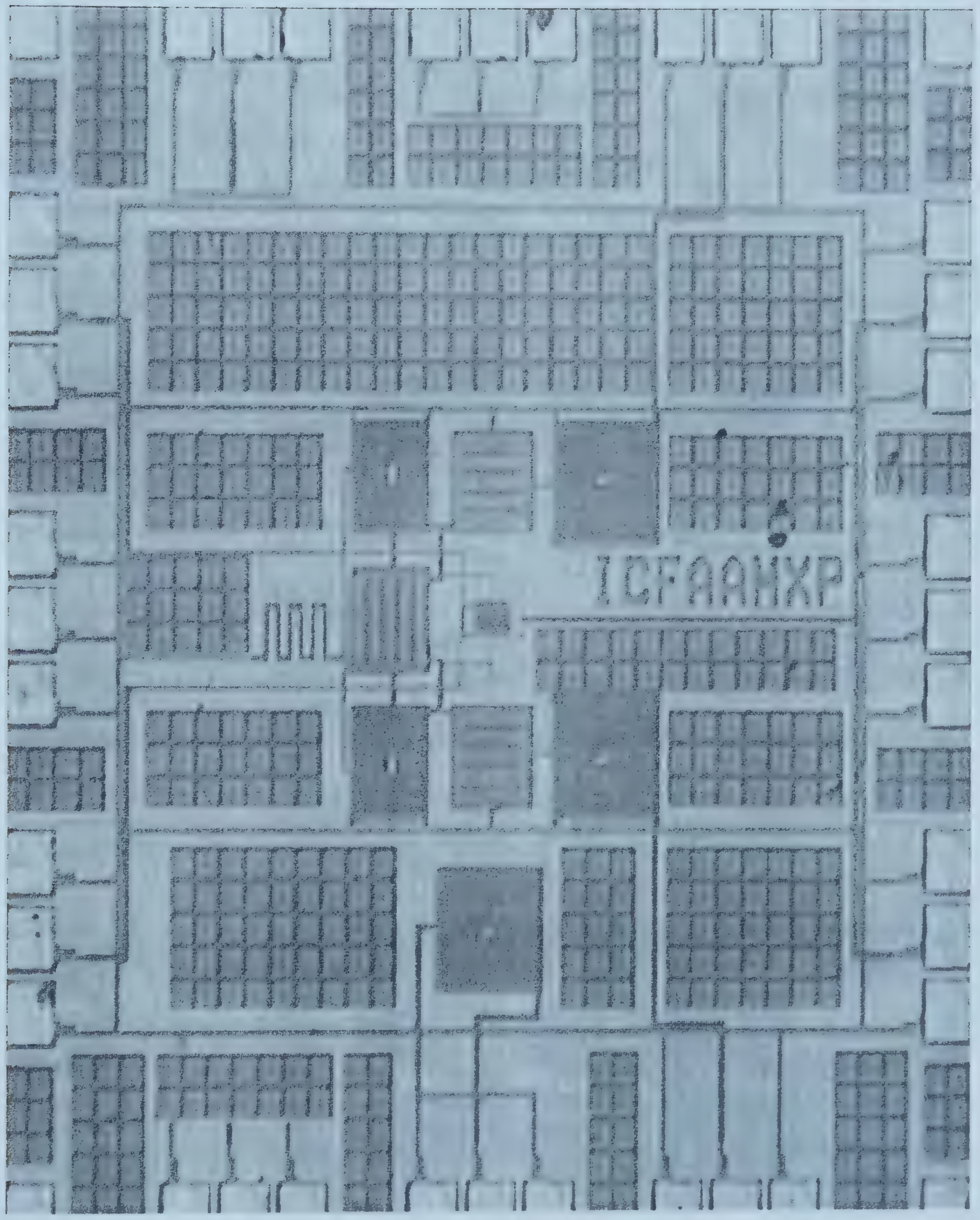


Figure 4-3: Die Photo of Experimental Switching Mixer.

Figure 4-3 shows a die photo of the switching mixer fabricated in 0.18µm CMOS technology.

4.1.2 Multiplying Mixer

The second experimental mixer is a down-conversion frequency mixer that bases its principle of operation on the multiplication of two signals. The classic Gilbert Multiplier Cell configuration with active loads was adopted for the design. A schematic showing the arrangement of the transistors and passive elements is included in Figure 4-4. All elements shown in the figure were designed with the intention of them being on-chip.

A resistor and a diode-connected transistor provide the primary bias circuitry. Resistor R_1 and transistor M11 maintain biasing of the whole circuit and establish how each of the transistors operate. The designed bias current flowing through transistor M11 was determined by solving (4.6) and (4.7) simultaneously. Using the values in Appendix A containing the parameters for 0.18µm CMOS transistors with a power supply of 1.8V, and considering that transistor M11 has dimensions of 10µm and 0.5µm for width and length, and using the expressions

$$I_{DS,M11} = \frac{1}{2}\mu_n C_{OX} \frac{W_{11}}{L_{11}} \left[V_{GS,M11} - V_{TN}\right]^2 . \tag{4.6}$$

$$V_{GS,M11} = Vdd - R_1 I_{DS,M11} . \tag{4.7}$$

The values of the R_1 and the drain-source current were determined to be 960Ω and 0.8µA.

Transistors M11 and M10 form a current mirror by having the gate terminals of both connected together. The designed drain-source current of M10 as determined by (4.8)

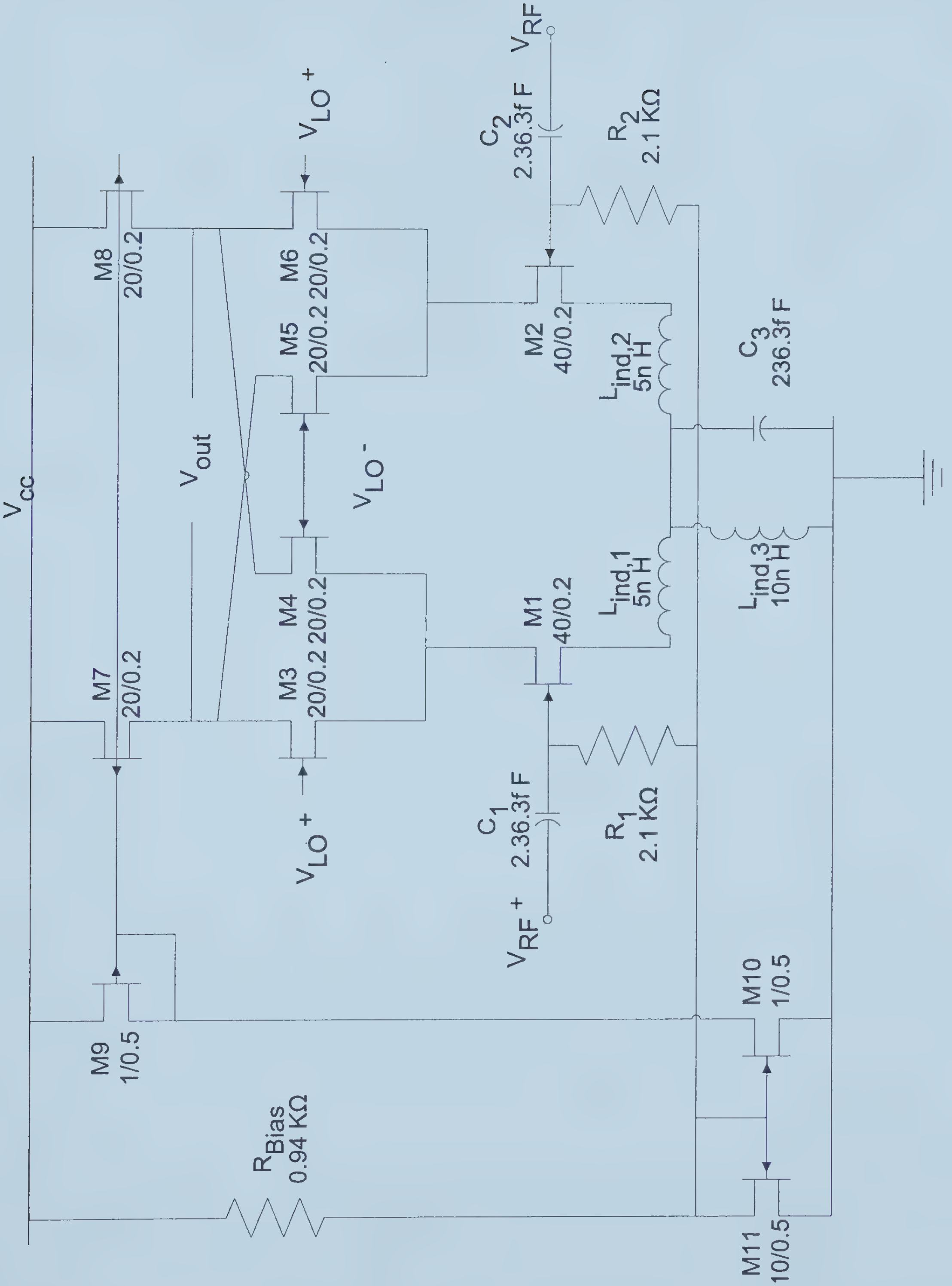


Figure 4-4: Schematic of Experimental Multiplying Mixer.

$$\frac{I_{DS,M11}}{I_{DS,M10}} = \frac{W_{M10}/L_{M10}}{W_{M11}/L_{M11}}. \tag{4.8}$$

is 80μA.

Since the diode-connected transistor M9 is in series with M10, the bias currents of M9 and M10 are identical. Bias currents for the transistors acting as active loads (M7 and M8) and voltage-current converters (M1 and M2) are established by having either their gate terminal connected to the gate terminal of M9 or M10. For instance, as the gate-source voltages of M9 and M7 are the same, the drain-source current of M9 is reproduced and multiplied by the ratio between the dimension of transistors M7 and M9 namely.

Transistor pair M9 and M10 are connected in series to prevent any events in which the current transistors M7 and M8 are different from transistors M1 and M2. With M9 and M10 connected in series, any variations in current will still result in the same bias current being supplied to the either the active loads or the voltage-current converters. In the instances when the gate terminal of either M_9 or M_{10} deviates from the designed values, this change in the gate voltage will result in a change in the bias current for either the active loads or current-voltage converters. The deviation from the bias gate voltage might lead to undesirable situations in which the current-voltage converters are operating in the active-region or the active loads operating in the constant current region.

Two extra features were added to the experimental frequency mixer—source-degeneration inductors and an inductor-capacitor tank. With the intended operating supply voltage being 1.8V, it was necessary to address the shortage of voltage headroom. To do this, an inductor-capacitor tank consuming zero voltage headroom was incorporated. The inductor-capacitor tank was designed with a resonant frequency of 3

GHz. An inductor of value 10nH and a capacitor of 281.4pF provide a resonant frequency of 3 GHz. However, when an extracted layout was performed using simulation software, the capacitor value was reported to be 236.3fF. Inductors were connected in series between the source terminal and the inductor-capacitor tank to maximize linearity with for two inductors having an impedance value of 95Ω at 3 GHz.

The approximated impedance values of the active loads were determined using for a bias current of 4mA and a length of 0.2μm. The impedance values presented by transistors M7 and M8 are both 800Ω, and calculated as

$$R_{on} = \frac{16L_{M7}}{I_{DS,M7}}. \tag{4.9}$$

With V_{DC} having a value of 1.05V and Z_L a value of 0.8KΩ, using the transistor parameters listed in Appendix along with (4.10), it can be determined that the designed voltage conversion gain for the experimental multiplying frequency mixer is

$$G = \frac{2\mu C_{OX}}{\pi}\frac{W_1}{L_1}\left(V_{DC} - V_{TN}\right)Z_L. \tag{4.10}$$

and is 9.95dB.

Figure 4-5 shows a die picture of the fabricated multiplying mixer. In the picture, two 5nH inductors and a 10nH are shown at the bottom half with all transistors located in the middle.

4.1.3 Design Summary

0.18μm CMOS technology available through the Canadian Microelectronic Centre (CMC) was selected for the fabrication process. CMOS technology was chosen to create an all CMOS RF front-end module that can be integrated with other high frequency

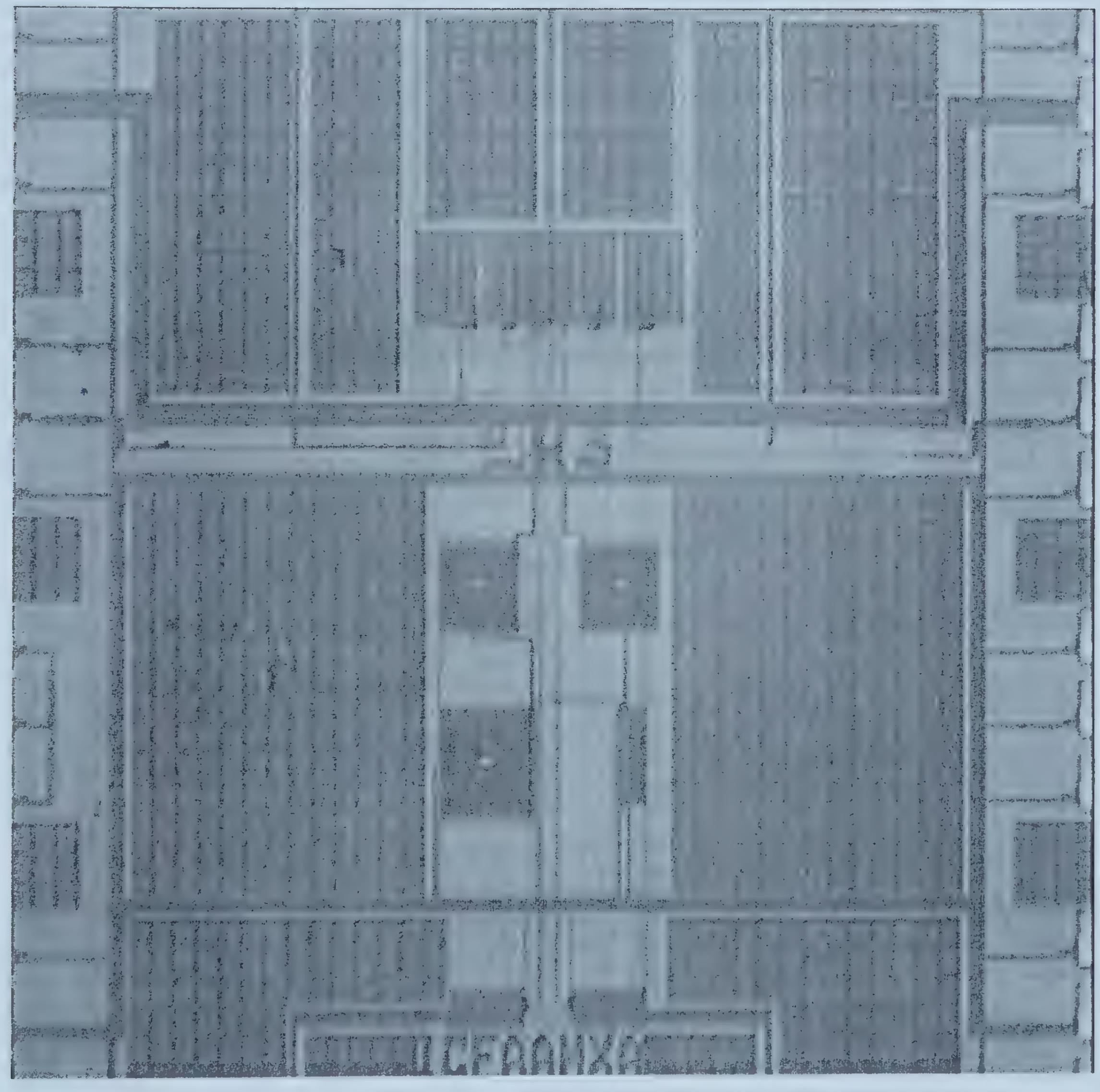


Figure 4-5: Die Photo of Experimental Multiplying Mixer.

analog and digital circuitry to form a single mobile telephony chip. The two experimental designs were first simulated using schematics to meet the necessary requirements. Simulations were then carried out in layout to ensure that performances of the mixers corresponded to the designed values. After both mixers were determined to be able to meet the requirements for 3G W-CDMA in simulation, fabrication was carried out by Taiwan Semiconductor Manufacturing Corporation (TSMC) via CMC.

4.2 Experimental Testing

The fabricated loose die mixer circuits were surface-mounted onto a 80-pin ceramic flat pack (CFP) with a square cavity that had 20 bonding fingers on each side. A printed circuit board test fixture available through CMC having twelve high frequency signal lines was chosen for the differential radio frequency and local oscillator inputs and the intermediate frequency output. As the inputs to both designs were differential, differential inputs were obtained by using power splitters and line stretches. Both radio frequency and local oscillator signals were applied to the input port of two separate two-way-0^0 power splitters, producing a pair of input radio frequency signals and a pair of local oscillator signals with the same phase. Delays using line stretchers were added to each signal of the two pairs resulting in a 180^0 phase shift and producing differential radio frequency and local oscillator inputs.

Equipment	*Manufacturer*	*Model*
Oscilloscope	Tektronix	7104
Signal Generator	Rohde & Schwarz	SMT03
Power Meter	Rohde & Schwarz	NRVS
Power Splitter	Mini Circuit	Z FSC-2-2500

Table 4-2: Equipments Used in Experimental Testing.

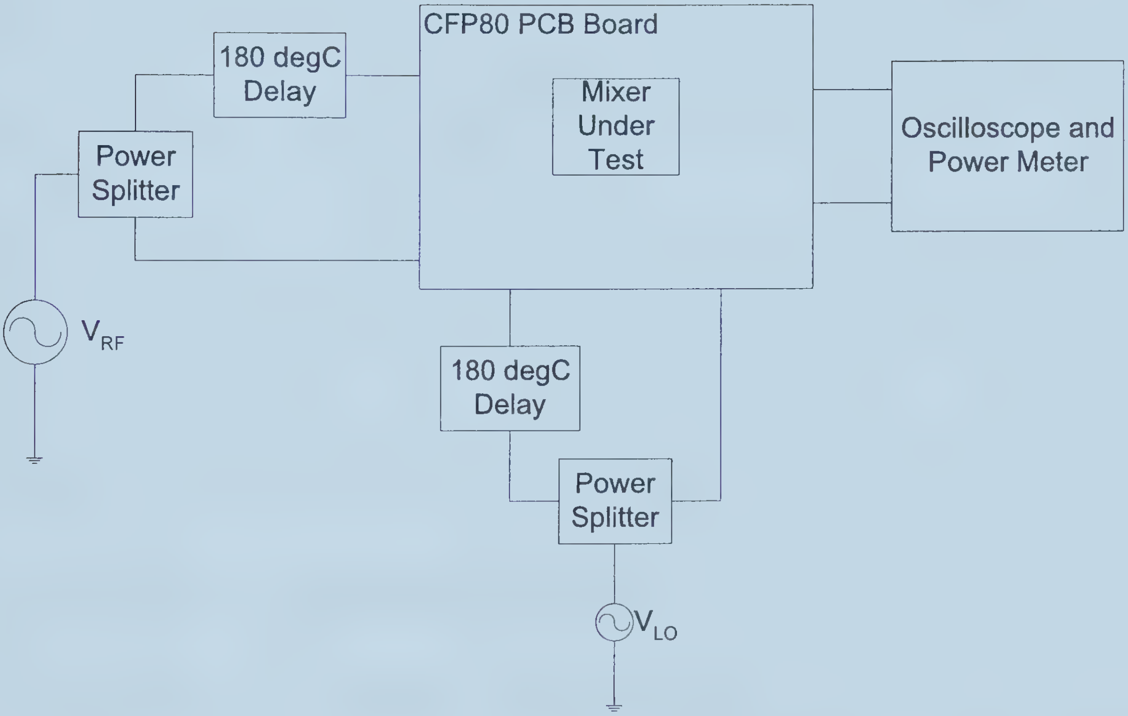


Figure 4-6: Block Diagram Showing Testing Setup.

All the mixer packages were clammed onto the printed circuit board with the equipments listed in Table 4-2 setup as shown in Figure 4-6. Two signal generators with a maximum frequency of 3 GHz were used to act as the radio frequency and the local oscillator signals. To measure the conversion gain, the frequencies of the two signal generators were set to 2.85 and 3 GHz representing the frequencies of the intended local oscillator and radio frequency signals. With the local oscillator signal set with a constant power level of 13.0dBm, the power level of signal generator acting as the input radio frequency signal was then varied with the output levels for the different input power levels being recorded.

The frequency of the signal generator acting as input radio frequency was then changed to 1.5 GHz and the power level of the signal generator was again varied with the output level being recorded. The change in the frequency was used to simulate the third order harmonic distortion that will determine a dynamic useable range on the frequency mixer.

4.3 Experimental Data and Discussion

4.3.1 Specification for Simulation and Experimentation

In both simulations and experimentation, two voltage signal sources acting as the local oscillator and radio signal were used. The desired input signal's frequency was set at 3 GHz with a desire to have the intermediate frequency output in the 150 MHz frequency spectrum. The frequency of the local oscillator was set to 2.85 GHz. With the power level of local oscillator signal held constant at 13dBm, the power level of the input signal was varied between 0dBm and 13dBm to measure the conversion gain in simulation and experimentation for both frequency mixer designs. With only the frequency of the input

signal changed to 1.5 GHz, the same process was repeated to measure the third order harmonic responses for both mixer designs.

4.3.2 Voltage Conversion Gain

Figure 4-7 shows the simulated conversion gain for both frequency mixer designs. On average, the switching frequency mixer has a voltage conversion gain of -1.33dB whereas the multiplying frequency mixer achieved a voltage conversion gain of 10.4dB at high input level. The simulated conversion gains of both mixer designs are both close to the theoretical expected values. At low input power level, the conversion gain of the multiplying frequency mixer is lower than expected; this is due to the harmonic distortion resulting in difficulty in obtaining accurate measurements. The better than expected conversion gain obtained for the switching frequency mixer is most likely caused by harmonic distortions that are presented as noise at the output, together with the intermediate frequency giving values that are better than theoretical ones.

Voltage conversion gain determined experimentally for the switching and multiplying mixers are shown in Figure 4-8. Experimentally, the switching mixer obtained a voltage conversion gain of -18.5dB while the multiplying mixer achieved -15.5dB in voltage conversion gain. The oscilloscope used in the measurements had an internal bandpass filter with centre frequency of 1 GHz. This feature in the oscilloscope facilitates the measurement of down-converted signals as most of the harmonic responses are filtered out. From Figure 4-8, it is clearly seen that the conversion gain for both experimental frequency mixers are constant but with lower conversion gain than predicted by theoretical calculation and the simulated data. This is most likely due to numerous factors.

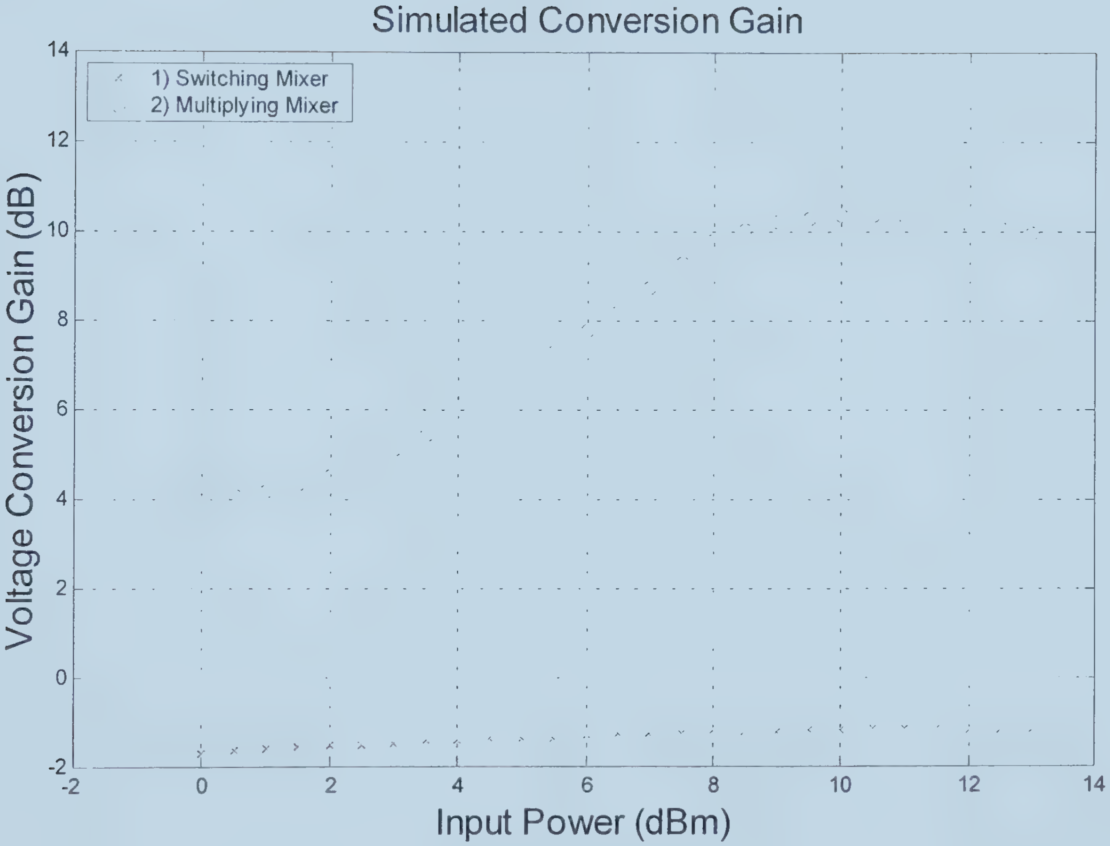


Figure 4-7: Simulated Voltage Conversion Gain.

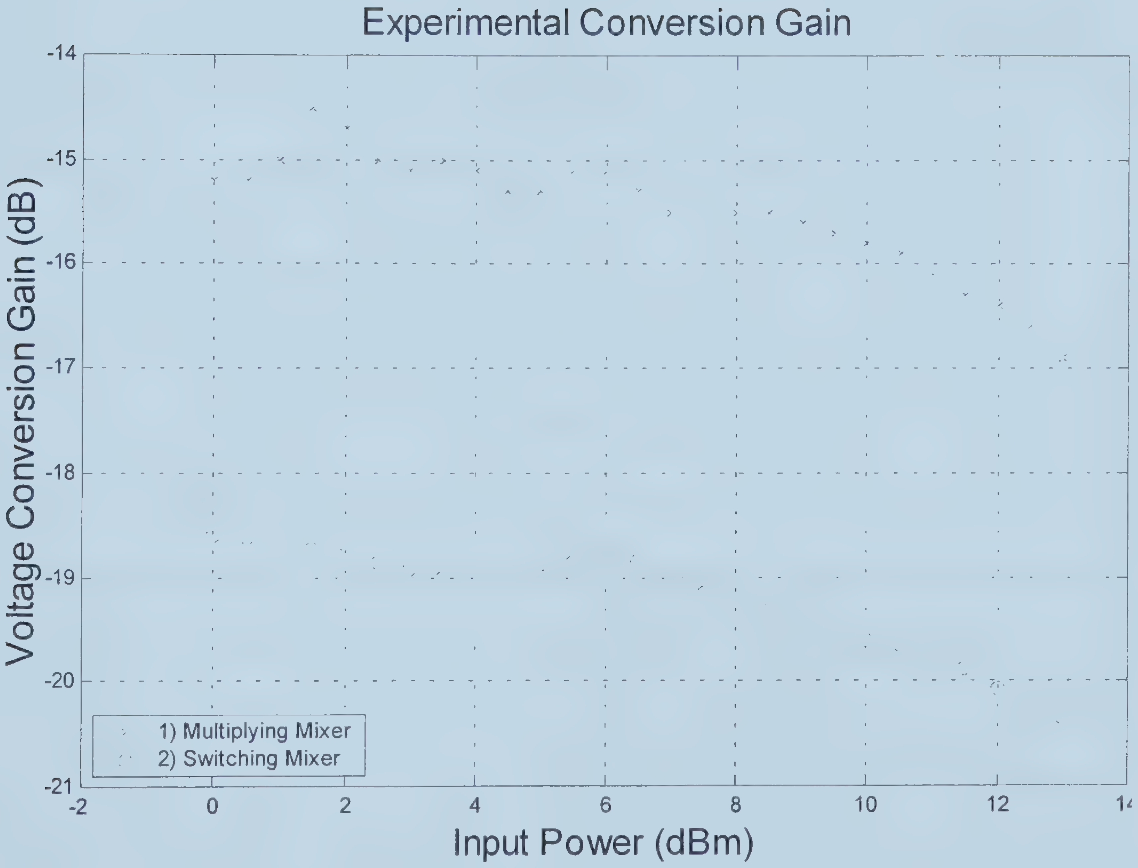


Figure 4-8: Experimental Voltage Conversion Gain.

Some factors—such as mismatch in input-output matching causing a reduction in the power transferred; power loss in the bonding pad and package; and the clamming of the package onto printed circuit boards—could have all contributed to lower than anticipated voltage conversion gains. At high input power level, the experimentally determined conversion gain for both frequency mixers show a decrease. The decline in conversion gain at high input power level is the direct consequence of the physical dynamic limits of the transistor. As the input power level is increased, the output level reaches a limit and ceases to increase proportionally, resulting in a lower conversion gain.

4.3.3 Input Third-Order Intercept Point

From the Fourier series expansion of a unit square wave, it can be seen that when a unit square wave is multiplied by the input sinusoidal signal, the presence of higher harmonic terms will produce an output with a frequency spectrum that is identical to the desired intermediate frequency signal, leading to distortion. In the hope of characterizing this distortion, the frequency of the input signal generator was changed from 3 GHz to 1.5 GHz. The change represents the effect of third-order harmonic distortion. In both simulation and experiment, the output power at both 3 GHz and 1.5 GHz for both frequency mixer designs was recorded as the input power level was varied. The outputs when the frequency of the input signal was 3 GHz represented the fundamental, whereas the outputs when the frequency was 1.5 GHz represented the third order distortion. The fundamental and third order distortion outputs were converted into power and plotted against the input power. In the plots, the fundamental output has a gradient of one, and the third order output has gradient of three.

Figure 4-9 shows the output power for the switching mixer design in simulation. Points

made up of “x” and “o” characters represent the actual measured values for the fundamental and third-order harmonic power levels respectively. Two straight lines with gradients of one and three were drawn to “best fit” these values. From Figure 4-9, the input third-order intercept point of the switching mixer is 10.5dBm and 12dBm for the output third-order intercept point. Both the fundamental and third-order experience the expected compression at high input power, with the 1dB compression input point occurring at about 9dBm in simulation. Figure 4-10 shows the output power obtained for the multiplying mixer design in simulation. Two straight lines with the gradients of one and three were drawn to “best fit” to determine the third-order intercept point and 1dB compression point. The input third-order intercept point for the multiplying mixer is 11dBm and a value of 23dBm is obtained for the output third-order intercept point while the 1dB compression point occurs at 11dBm.

Experimental output power measurements for the switching frequency mixer are shown in Figure 4-11. Two straight lines with gradients of one and three were used to “best fit” the points made up of “x” and “o” characters. The “x” points represent the measured values for the fundamental output and the “o” points represent the measured values for the third-order harmonic output. 10dBm and -8dBm in input and output referred third-order intercept points were obtained experimentally, and the 1dB compression point for the switching frequency mixer was measured to occur at 8dBm.

Output power measurements determined experimentally for the multiplying mixer are shown in Figure 4-12. Two straight lines with gradients of one and three were drawn to “best fit” to determine the third-order intercept point and 1dB compression point. The third-order intercept point for the multiplying mixer is 14.5dBm when referred to the

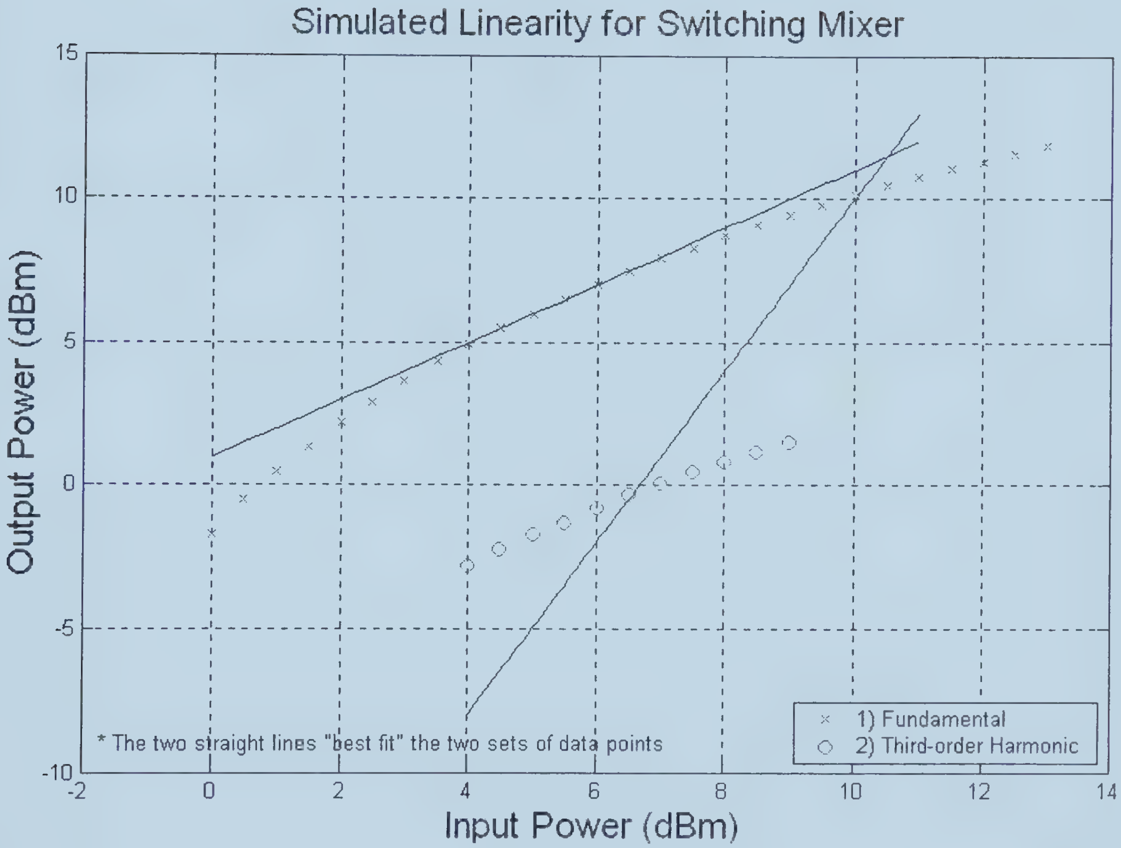


Figure 4-9: Simulated Linearity for Switching Mixer.

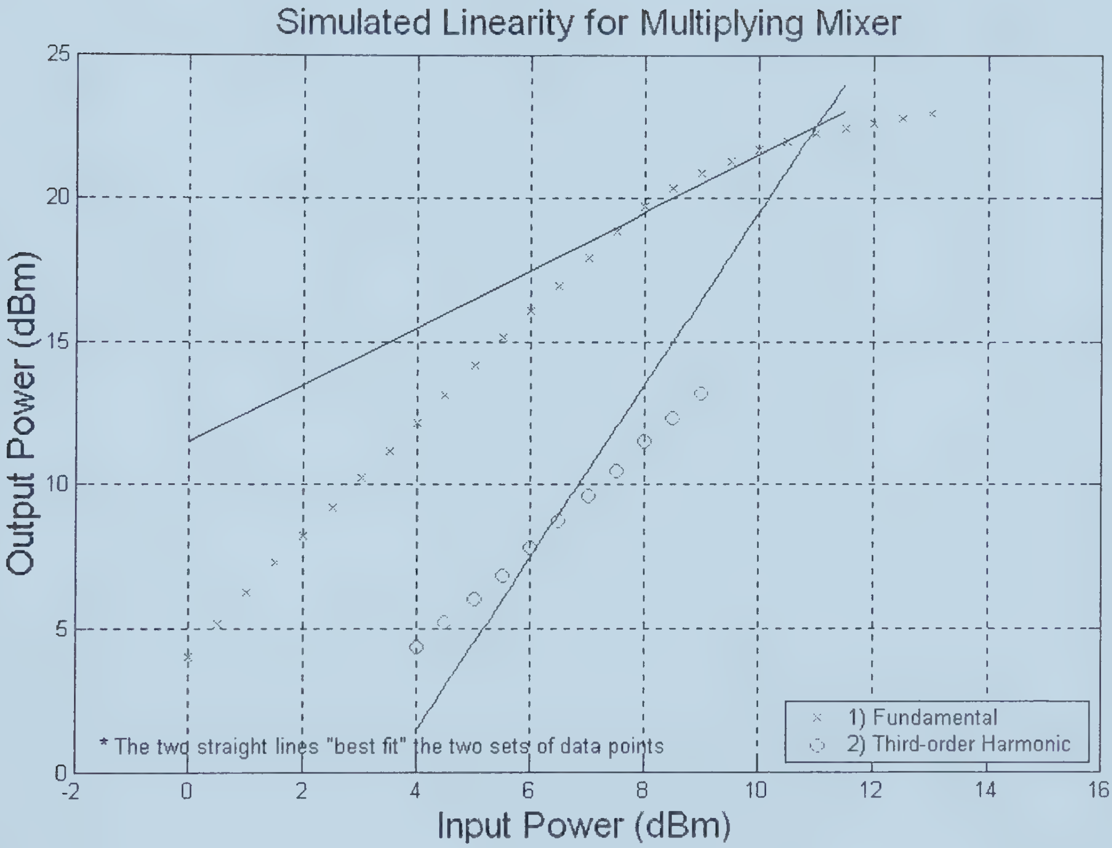


Figure 4-10: Simulated Linearity for Multiplying Mixer.

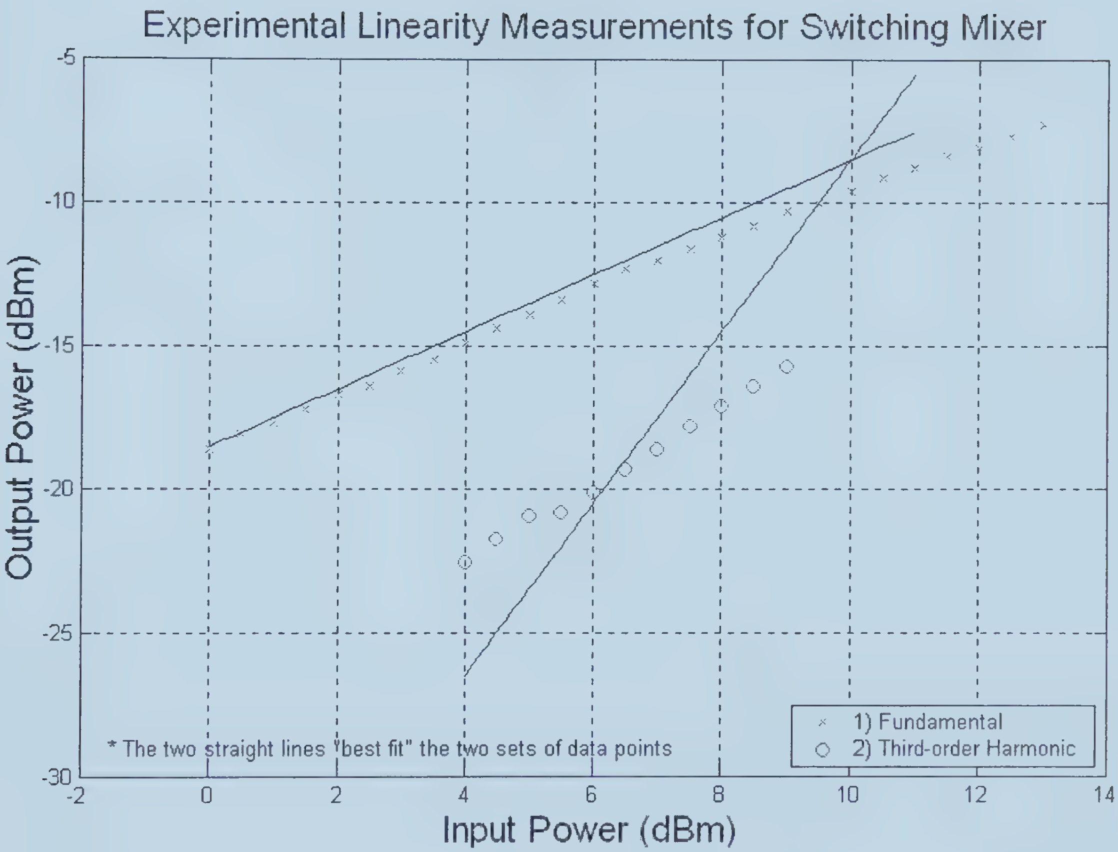


Figure 4-11: Experimental Linearity for Switching Mixer.

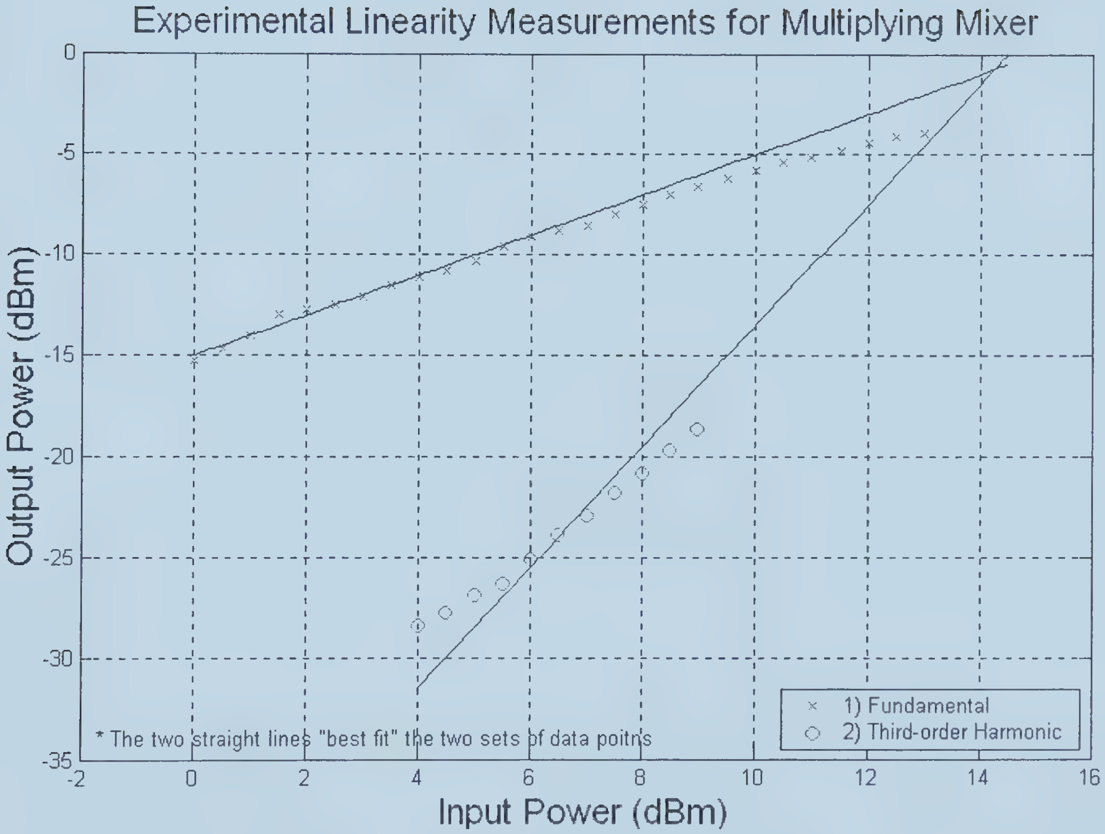


Figure 4-12: Experimental Linearity for Multiplying Mixer.

input and a value of -2dBm is obtained when referred to the output. The 1dB compression point for the multiplying frequency mixer occurs at 10dBm.

4.3.4 Simulation and Experimental Results

	Theoretical	Simulation	Experimental
LO Frequency (GHz)		2.85	2.85
LO Power Level (dBm)		13.0	13.0
Voltage Conversion Gain (dB)	-9.94	-1.33	-18.5
Input-IP3 (dBm)		10.5	10
Output-IP3 (dBm)		12	-8
1dBCompression (dBm)		9	8
Technology			0.18μm CMOS
Die Area (mm2)			1.00

Table 4-3: Switching Frequency Mixer Performance.

	Theoretical	Simulation	Experimental
LO Frequency (GHz)		2.85	2.85
LO Power Level (dBm)		13.0	13.0
Voltage Conversion Gain (dB)	9.95	10.4	-15.5
Input-IP3 (dBm)		11	14.5
Output-IP3 (dBm)		23	-2
1dBCompression (dBm)		11	10
Technology			0.18μm CMOS
Die Area (mm^2)			4.84

Table 4-4: Multiplying Frequency Mixer Performance.

Table 4-3 summarizes the data for the switching frequency mixer while Table 4-4 summarizes the data for the multiplying frequency mixer. The figures and tables in this chapter show promise that it is possible to build third generation cellular telephony radio

frequency front-end modules using 0.18µm CMOS technology and that meet the requirements set forth for W-CDMA. In both CMOS mixers, the conversion gains obtained in simulation validated the theoretical analysis. However, the experimental conversion gains for both mixers differed from the theoretical analysis. A lower current density for the metal layer used, as well as parasitic capacitances, mismatched input-output matching, and harmonic distortion all contributed to a lower than intended conversion gain. Nevertheless, the data acquired for both frequency mixer designs showed what was expected functionally—a consistent voltage conversion gain for a range of input power levels.

From the figures showing the fundamental and third-order power outputs, both frequency mixers behave as anticipated. With the frequency of the input signal set at 3 GHz and the output power plotted against the input power level, the "best-fit" straight line for the output power graphs showed a gradient of one for both frequency mixers. Input and output third-order intercept points could not be determined theoretically, as the exact polynomial equations characterizing the transistors were not known. The third-order intercept points were determined in simulation and used as points of reference.

Input third-order intercept points for both frequency mixer designs exhibited very close correlation between simulation and experimentation. From simulation, the switching frequency mixer achieved 10.5dBm while the multiplying frequency mixer obtained 11dBm. These values were validated via experimentation with 10dBm and 14.5dBm for the switching and multiplying frequency mixers respectively.

However, the output third-order intercept points obtained in experimentation differed from the simulation results. A difference of more than 20dBm exists between the results

acquired in simulation and experimentation for both frequency mixer designs. In simulation, the switching frequency mixer had 12dBm for the output third-order intercept point but -8dBm was achieved in experimentation. For the multiplying frequency mixer, an output third-order intercept point of 23dBm was attained in simulation, in contrasts to the -2dBm achieved through experimentation. The huge difference between the simulated and experimental results in the output third-order intercept points could only be explained by the low conversion gain obtained experimentally. With the lower gain, the linearity plots for the experimental values are shifted down vertically, giving a lower output third-order intercept point in both frequency mixer designs.

Both frequency mixers exhibited close correlation between simulation and experimentation in the 1dB compression point. The switching frequency mixer design achieved a compression point of 9dBm in simulation and from experiments a compression point of 8dBm was attained. 11dBm in compression point was acquired in simulation for the multiplier-based frequency mixer design; from the experiments carried out on the fabricated silicon chips, a 1dB compression point of 10dBm was achieved.

From the data gathered, both frequency mixer designs achieved the anticipated conversion gain in simulations; however due to physical deficiencies of devices used, the conversion gains obtained were significantly lower than the calculated and simulated values. Linearity of both mixer designs were first simulated and the data acquired showed that the third-order intercept points and 1dB compression points obtained in simulation were validated from experimentation done on the fabricated silicon chips. These data obtained from experimentation corresponded closely with the simulated results except for the output third-order intercept points for both frequency mixer designs.

Chapter 5

5.0 Summary and Review of Results

The previous chapters presented two different architectures of frequency mixers intended for next-generation wireless communications—third-generation cellular systems and Bluetooth. Both designs were designed, simulated, and fabricated in a 0.18μm CMOS technology environment with the hope of creating a single transceiver microchip that incorporates a radio-frequency front end, digital-analog converters and digital circuitry.

In the first design, four transistors made compromised the core of a frequency mixer that operated using the principle of multiplying the input signal with a unit square wave generated by switching transistors on and off. The second design took on a Gilbert Multiplier Cell that had six transistors at the core of frequency translation. This frequency mixer operated with the principal of multiplying the input radio frequency signal with the local oscillator signal to produce the mixing effect. Comparing performance metrics such as conversion gain, third-order intercept, and 1dB points, theoretical analysis and simulated results showed that the performance of the multiplier-based mixer was superior to that of the switching frequency mixer.

However, the fabricated microchips of both designs did not perform as well as predicted by the theoretical analysis or the simulation results; this was especially true for the conversion gain. On the other hand, functionally both sets of microchips yielded the anticipated characteristics and performed well from a functional standpoint; the

conversion gain stayed relatively constant at low input power level and as the input power level in increased, the conversion gain started to decrease and level off.

The switching frequency mixer design suffered from mismatch in the sizes of transistors. In both simulation and experimentation, the output power recorded in both situations with the frequency of input source changed to 1.5 GHz show a gradient of closer to two instead of the expected of three.

During the course of the work for this thesis, the objective was met. Namely, the thesis objective was to determine if it is possible to build front-end RF modules with new CMOS technology having a lower available power supply while meeting the stricter requirements. Aside from the lower than expected conversion gain, both theoretical analysis and simulation results support the idea of fully integrated wireless transceiver microchips using 0.18μm CMOS technology that encompass front-end RF modules, Analog-Digital converters, and digital modulation/demodulation circuitry.

5.1 Further Research

The lower than anticipated conversion gains obtained from experimentation for both frequency mixer designs are the results of various factors, such as the presence of parasitic capacitances and inductances that are absent in both theoretical analysis and simulation, power loss in mismatch of the input and output, and harmonic distortion. The influence of these factors could most likely be minimized or removed by careful design.

Transformers fabricated with the use of CMOS technology together with the transistors on the microchip should be used to convert single-ended signals from the signal generator to differential-ended signals providing a truly differential pair to the mixer circuits. This would reduce any errors that might be associated with the use of line stretchers. As for

the differential intermediate output, a differential-pair to single-ended converter should also be employed.

The use of line stretchers reduced the accuracy of any analysis on isolation between any two ports. With the elimination of line stretchers, any analysis done on the performance metric of isolation will show how well the ports are isolated from each other and indicate if any filters are necessary. Besides the lack of isolation analysis, two other performance metrics were absent.

Analysis and comparison of the mixers based on noise figure was not carried out due to the absence of noise generators at the local facilities. Further research such as the analysis of noise figure and power consumption should be carried out to yield the minimum signal to noise ratio, maximum power consumption, and average power consumption. Data acquired for noise figure and power consumption could then be combined with the data obtained for conversion gain and linearity to make for a better comparison between the two designs. With the data for the performance metrics—conversion gain, linearity, noise figure, and power consumption—it could then be determined if the two frequency mixers meet the necessary requirements for 3G W-CDMA mobile telecommunications.

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Appendix

	N-type	P-Type
V_{TO} (V)	0.4	-0.48
μC_{OX} ($\mu A/V^2$)	190	47
E_{SAT} (V/μm)	4.54	8.46
L_{CRIT} (for 1.8V power supply) (μm)	0.62	0.31
t_{OX} (m)	$4.1*10^{-9}$	$4.2*10^{-9}$
C_{OX} ($8.54*10^{-3}$ pF/μm^2)	8.54	8.33
R_{ON} (KΩ)	$\frac{16{,}000L}{I}$	$\frac{26{,}000L}{I}$

Table A: MOS Parameters for a Typical 0.18μm CMOS Technology